Agustín Navarro-Torres

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Summary

I am a Postdoctoral Researcher at the University of Murcia under the supervision of Professor Alberto Ros. My research focuses on microarchitecture, with expertise in Memory Hierarchy (MSHR design, hardware data prefetching including the Berti prefetcher, and cache management), Branch Target Buffer optimization, and performance characterization of real-world hardware. Previously, I earned my PhD at the University of Zaragoza and briefly worked as a Visiting Researcher at Huawei's Research Center, Zürich.

Education

University of Zaragoza *PhD in Computer Science* *2018 – 2023*

- **Thesis:** Contributions to High—Performance Memory Hierarchies: Program Characterization, Resource Control, Transactional Synchronization, and Hardware Prefetching.
- **Supervisor:** Pablo Ibáñez & Jesús Alastruey—Benedé.

University of Zaragoza *MSc in Computer Science* *2016 – 2018*

- **Thesis:** Memory characterization of the SPEC CPU2017 Benchmark Suite.
- **Supervisor:** Pablo Ibáñez.

University of Zaragoza *BS in Computer Science* *2012 – 2016*

- **Thesis:** Design and evaluation of cache memories for a multicore chip powered at very low voltage.
- **Supervisor:** Pablo Ibáñez.

Experience

Postdoctoral Researcher *Universidad de Murcia, Spain* *2024 –*

- **Supervisor:** Alberto Ros.
- Develop research in the following areas: Memory Hiearchy (MSHR & Caches), Data Hardware Prefetching, Branch Target Buffers (BTB) and Branch Predictor….

Research Intern *Huawei Research Center, Zürich, Switzerland* *Sept. 2020 – Feb. 2021*

- **Supervisor:** Maria Carpe—Amarie.
- Characterization of Multiple Synchronization Mechanisms.
- Development of a hardware mechanism to reduce the number of storage replacements in a Simultaneous Multithreading (SMT) environment.

Research Intern *Universidad de Murcia, Spain* *Sept. 2021 – Dec. 2021*

- **Supervisor:** Alberto Ros
- Development of a new Data Hardware Prefetcher.

Publications

Berti: an Accurate Local-Delta Data Prefetcher, *Agustín Navarro-Torres*, Biswabandan Panda, J. Alastruey-Benedé, Pablo Ibáñez, Víctor Viñals-Yúfera, and Alberto Ros. 55th International Symposium on Microarchitecture (MICRO), 2022. IEEE

Secure Prefetching for Secure Cache Systems, Sumon Nath, *Agustín Navarro-Torres*, Alberto Ros, and Biswabandan Panda. 57th International Symposium on Microarchitecture (MICRO), 2024. PDF

A Complexity-Effective Local Delta Prefetcher, *Agustín Navarro-Torres*, Biswabandan Panda, J. Alastruey-Benedé, Pablo Ibáñez, Víctor Viñals-Yúfera, and Alberto Ros. IEEE Transactions on Computers, 2024. IEEE

BALANCER: Bandwidth Allocation and Cache Partitioning for Multicore Processors, *Agustín Navarro-Torres*, J. Alastruey-Benedé, Pablo Ibáñez, and Víctor Viñals-Yúfera. Journal of Supercomputing, 2022, Springer Link

Synchronization Strategies on Many-Core SMT Systems, *Agustín Navarro-Torres*, Maria Carpe-Amarie, J. Alastruey-Benedé, Pablo Ibáñez, and Víctor Viñals-Yúfera. 33rd International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), 2021 IEEE

Memory hierarchy characterization of SPEC CPU2006 and SPEC CPU2017 on the Intel Xeon Skylake-SP, *Agustín Navarro-Torres*, Maria Carpe-Amarie, J. Alastruey-Benedé, Pablo Ibáñez, and Víctor Viñals-Yúfera. PLOS ONE, 2019 PLOS ONE

Exposing Abstraction-Level Interactions with a Parallel Ray Tracer, Darío Suárez Gracia, Ruben Gran Tejero, Luis M. Ramos, *Agustín Navarro-Torres*, Adolfo Muñoz, Joaquín Ezpeleta, José Luis Briz, Ana C. Murillo, Eduardo Montijano, Javier Resano, María Villarroya-Gaudó, Jesús Alastruey-Benedé, Enrique Torres, Pedro Álvarez, Pablo Ibáñez, and Víctor Viñals. Workshop on Computer Architecture Education (WCAE), 2019 PDF

Reviewer

During my research career, I have served as a reviewer for several journals and conferences, including as an Artifact Reviewer for the *International Symposium on Microarchitecture (MICRO)*.

Grants

- **Doctoral Grant** (FPI) from the Ministry of Science and Innovation, 4.5 years.
- **Mobility Grant for Internships** ("Ayudas a la movilidad predoctoral para la realizaci'on de estancias breves en Centros de I+D"), Universidad de Zaragoza, 4 months.

Awards

- 2022 & 2024 EU HiPEAC paper award for publication in the most prestigious venues.

Teaching

- *"Ampliación de Estructura de Computadores"*, BSc. Computer Science, Universidad de Murcia, (2024/2025).
- *"Fundamento de Computadores"*, BSc. Computer Science, Universidad de Murcia, (2024/2025).
- *"Sistemas Distribuidos"*, BSc. Computer Science, Universidad de Murcia, (2023/2024).
- *"Estructura y Tecnología de Computadores"*, BSc. Computer Science, Universidad de Murcia, (2023/2024).
- TA in *"Computación de Altas Prestaciones"*, MSc. Computer Science, Universidad de Zaragoza, (2022/2023).
- TA in *"Sistemas Operativos"*, BSc. Computer Science, Universidad de Zaragoza, (2022/2023).
- TA in *"Procesadores Comerciales"*, BSc. Computer Science, Universidad de Zaragoza, (2020 — 2022).

Undergraduate Thesis Supervisor:

- *"Integrating ChampSim Prefetchers into Gems4Proc"*, Simranjit Singh Kaur, Universidad de Murcia, (2024).
- *"Estudio de puntualidad en el prebuscador Berti"*, Hernan Rodolfo Salambay Roldan, Universidad de Murcia, (2024).