Alberto Ros

- RESUME -
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ADDRESS

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RESEARCH INTERESTS

Broad Category:	Computer Architecture, Multiprocessor Architecture.
Specific Areas Include:	Multicore and manycore architectures, Cache coherence protocols, Memory systems, Cache hierarchy, Memory models, Performance evaluation.

PROFESIONAL EXPERIENCE

May'13 – nowadays	Associate professor Facultad de Informática – Universidad de Murcia
Jan'12 – Apr'13	Ph.D Assistant professor Facultad de Informática – Universidad de Murcia
Aug'11 – Jan'12	Postdoctoral researcher Department of Information Technology – Uppsala University
Dec'10 – Sep'11	Adjunct professor (part-time) Facultad de Informática – Universidad de Murcia
Oct'09 – Aug'11	Postdoctoral researcher Escuela Técnica Superior de Informática – Universidad Politécnica de Valencia
Sept'04 – Sept'09	Research Assistant Facultad de Informática – Universidad de Murcia

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EDUCATION

Sept'04 – Sept'09	Ph. D. Computer Science (September, 2009) Facultad de Informática – Universidad de Murcia Dissertation Title: "Efficient and Scalable Cache Coherence for Many-Core Chip Multiprocessors" Advisors: José M. García and Manuel E. Acacio
Sept'99 – Jul'04	M.S., Computer Science (July, 2004) Facultad de Informática – Universidad de Murcia

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FELLOWSHIPS AND AWARDS

2015	HiPEAC paper award – ISCA'15 Given by HiPEAC (European Network of Excellence on High Performance and Embedded Architectures and Compilation).
2015	HiPEAC paper award – HPCA'15
2013	HiPEAC paper award – ISCA'13
2011	HiPEAC paper award – ISCA'11
2010	Spotlight paper in the IEEE TPDS.
Jul'08 – Sept'08	3-months collaboration at the University of Edinburgh. Granted by HiPEAC.
Apr'04 – March'09	Pre-doctoral Fellowship (Beca FPU de Formación de Profesorado Universitario). Granted by MEC (Spanish Ministry of Education and Culture).

INTERNSHIPS

Sep'15 – Dec'15	Visiting researcher at Uppsala University. Duration: 16 weeks.
Sep'14 – Dec'14	Visiting researcher at Uppsala University. Duration: 17 weeks.
Oct'13 – Dec'13	Visiting researcher at Uppsala University. Duration: 10 weeks.
Oct'12 – Dec'12	Visiting researcher at Uppsala University. Duration: 11 weeks.
Jul'08 – Aug'08	Internship at the University of Edinburgh. Duration: 2 weeks.
Jul'08 – Oct'08	Internship at the University of Edinburgh.

Duration: 16 weeks.

PUBLICATIONS AND IMPACT

Summary:

- Author of the book "Efficient and Scalable Cache Coherence for Chip Multiprocessors: Novel Proposals for Managing Cache Coherence in Future Many-Core Chip Multiprocessors". LAP Lambert Academic Publishing, February 2010.
- Editor of the book "Parallel and Distributing Computing". IN-TECH, January 2010.
- 26 publications in international conferences (including 3 in ISCA and 1 in HPCA), 11 international journal publications (including 2 in IEEE TPDS and 3 in IEEE TC), 1 book chapter, 4 international workshops, and 5 poster presentations.
- More than 370 citations according to GoogleScholar with an H-index of 10.

International conferences:

- Alberto Ros, Manuel E. Acacio, and José M. García, "A Novel Lightweight Directory Architecture for Scalable Shared-Memory Multiprocessors". 11th International Euro-Par Conference, pp. 582--591, August/September 2005. (Acceptance ratio 31,18%)
- Alberto Ros, Manuel E. Acacio, and José M. García, "An Efficient Cache Design for Scalable Glueless Shared-Memory Multiprocessors". ACM International Conference on Computing Frontiers, pp. 321--330, May 2006. (Acceptance ratio 25,0%)
- Alberto Ros, Manuel E. Acacio, and José M. García, "Direct Coherence: Bringing Together Performance and Scalability in Shared-Memory Multiprocessors". 14th Int'l Conference on High Performance Computing (HiPC), pp. 147--160, December 2007. (Acceptance ratio 20.55%)
- Alberto Ros, Manuel E. Acacio, and José M. García, "DiCo-CMP: Efficient Cache Coherency in Tiled CMP Architectures". 22nd IEEE International Parallel & Distributed Processing Symposium (IPDPS), pp. 1--11, April 2008. (Acceptance ratio 25.61%)
- Alberto Ros, Manuel E. Acacio, and José M. García, "Scalable Directory Organization for Tiled CMP Architectures". International Conference on Computer Design (CDES), pp. 112--118, July 2008. (Acceptance ratio 27%)
- Alberto Ros, Manuel E. Acacio, and José M. García, "Dealing with Traffic-Area Trade-Off in Direct Coherence Protocols for Many-Core CMPs". International Conference on Advanced Parallel Processing Technologies (APPT), pp. 11--27, August 2009. (Acceptance ratio 47.36%)
- Alberto Ros, Marcelo Cintra, Manuel E. Acacio, and José M. García, "Distance-Aware Round-Robin Mapping for Large NUCA Caches". 16th International Conference on High Performance Computing (HiPC), December 2009. (Acceptance ratio 18.77%)
- Alberto Ros, Blas Cuesta, Ricardo Fernández-Pascual, Maria E. Gómez, Manuel E. Acacio, Antonio Robles, José M. García, and José Duato, "EMC²: Extending Magny-Cours Coherence for Large-Scale Servers". 17th International Conference on High Performance Computing (HiPC), December 2010. (Acceptance ratio 19.2%)

- Blas Cuesta, Alberto Ros, Maria E. Gómez, Antonio Robles, and José Duato, “Increasing the Effectiveness of Directory Caches by Deactivating Coherence for Private Data ”. To appear in 38th International Conference on Computer Architecture (ISCA), June 2011. (Acceptance ratio 19.23%)

- Antonio García-Guirado, Ricardo Fernández-Pascual, Alberto Ros, José M. García, "Energy-Efficient Cache Coherence Protocols in Chip-Multiprocessors for Server Consolidation". 40th International Conference on Parallel Processing (ICPP), pages 51--62, Taipei (Taiwan), September 2011. (Acceptance ratio 22.31%)

- Antonio García-Guirado, Ricardo Fernández-Pascual, Alberto Ros, José M. García, "DAPSCO: Distance-Aware Partially Shared Cache Organization". 7th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC), Paris (France), January 2012.

- Alberto Ros, Polychronis Xekalakis, Marcelo Cintra, Manuel E. Acacio, José M. García, "ASCIB: Adaptive Selection of Cache Indexing Bits for Reducing Conflict Misses". International Symposium on Low Power Electronics and Design (ISLPED), pages 51--56, Redondo Beach, CA (USA), July 2012. (Acceptance ratio 15.92%)

- Stefanos Kaxiras, Alberto Ros, "Efficient, Snoopless, SoC Coherence". 25th IEEE International System-on-Chip Conference (IEEE SOCC), pages 230--235, Niagara Falls, NY (USA), September 2012. (Acceptance ratio 41.46%)

- Alberto Ros, Stefanos Kaxiras, "Complexity-Effective Multicore Coherence". 21st International Conference on Parallel Architectures and Compilation Techniques (PACT), pages 241--252, Minneapolis, MN (USA), September 2012. (Acceptance ratio 18.84%).

- Alberto Ros, Ricardo Fernández-Pascual, Manuel E. Acacio, "Using Heterogeneous Networks to Improve Energy Efficiency in Direct Coherence Protocols for Many-Core CMPs". 24th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), pages 43--50, Columbia University, NY (USA), October 2012. (Acceptance ratio 28.35%)

- Stefanos Kaxiras, Alberto Ros, "A New Perspective for Efficient Virtual-Cache Coherence". 40th International Symposium on Computer Architecture (ISCA), pages 535--547, Tel-Aviv (Israel), June 2013. (Acceptance ratio 19.44%)

- José L. Abellán, Alberto Ros, Juan Fernández, Manuel E. Acacio, "ECONO: Express Coherence Notifications for Efficient Cache Coherency in Many-Core CMPs". XIII International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pages 237--244, Samos (Greece), July 2013. (Acceptance ratio 47.62%)

- Alberto Ros, Blas Cuesta, María E. Gómez, Antonio Robles, José Duato, "Temporal-Aware Mechanism to Detect Private Data in Chip Multiprocessors". 42nd International Conference on Parallel Processing (ICPP), pages 562--571, Lyon (France), October 2013. (Acceptance ratio 30.57%)

- Alberto Ros, Mahdad Davari, Stefanos Kaxiras, "Hierarchical Private/Shared Classification: the Key to Simple and Efficient Coherence for Clustered Cache Hierarchies". 21st Symposium on High Performance Computer Architecture (HPCA), pages 186--197, Bay area, CA (USA), February 2015. (Acceptance ratio 22.57%)

- Joan J. Valls, Julio Sahuquillo, Alberto Ros, María E. Gómez, "The Tag Filter Cache: An Energy-Efficient Approach". 23rd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP), Turku (Finland), March 2015.
- Alberto Ros, Alexandra Jimborean, "A Dual-Consistency Cache Coherence Protocol". 29th International Parallel & Distributed Processing Symposium (IPDPS), pages 1119--1128, Hyderabad (India), May 2015. (Acceptance ratio 21.77%)
- Alberto Ros, Stefanos Kaxiras, "Callback: Efficient Synchronization without Invalidation with a Directory Just for Spin-Waiting". 42nd International Symposium on Computer Architecture (ISCA), pages 427--438, Portland, OR (USA), June 2015. (Acceptance ratio 19.02%)
- Stefanos Kaxiras, David Klaftenegger, Magnus Norgren, Alberto Ros, Konstantinos Sagonas, "Turning Centralized Coherence and Distributed Critical-Section Execution on their Head: A New Approach for Scalable Distributed Shared Memory". 24th International Symposium on High-Performance Parallel and Distributed Computing (HPDC), Portland, OR (USA), June 2015. (Acceptance ratio 16.38%)
- Mahdad Davari, Alberto Ros, Erik Hagersten, Stefanos Kaxiras, "An Efficient, Self-Contained, On-Chip, Directory: DIR1-SISD". 24nd International Conference on Parallel Architectures and Compilation Techniques (PACT), pages 317--330, San Francisco, CA (USA), October 2015. (Acceptance ratio 21.23%)

International journals:

- Alberto Ros, Ricardo Fernández, Manuel E. Acacio and José M. García, “Two Proposals for the Inclusion of Directory Information into the Last-Level Private Caches of Glueless Shared-Memory Multiprocessors”. Journal of Parallel and Distributed Computing (JPDC), 68 (11), pp. 1413--1424, November 2008.
- Alberto Ros, Manuel E. Acacio, José M. García, "A Scalable Organization for Distributed Directories". Journal of Systems Architecture (JSA), 56 (2-3), pp. 77--87, March 2010.
- Alberto Ros, Manuel E. Acacio, José M. García, "A Direct Coherence Protocol for Many-Core Chip Multiprocessors". IEEE Transactions on Parallel and Distributed Systems (TPDS), 21 (12), pp. 1779--1792, December 2010. *Spotlight paper*
- Antonio García-Guirado, Ricardo Fernández-Pascual, Alberto Ros, José M. García, "DAPSCO: Distance-Aware Partially Shared Cache Organization". ACM Transactions on Architecture and Code Optimization (TACO), vol. 8 (4), pages 25:1--25:19, January 2012.
- Alberto Ros, Blas Cuesta, Ricardo Fernández-Pascual, Maria E. Gómez, Manuel E. Acacio, Antonio Robles, José M. García, and José Duato, “Extending Magny-Cours Cache Coherence”. . IEEE Transactions on Computers (TC), vol. 61 (5), pages 593--606, May 2012.
- Blas Cuesta, Alberto Ros, María E. Gómez, Antonio Robles, José Duato, "Increasing the Effectiveness of Directory Caches by Avoiding the Tracking of Non-Coherent Memory Blocks". IEEE Transactions on Computers (TC), vol. 62 (3), pages 482--495, March 2013.
- Joan J. Valls, Alberto Ros, Julio Sahuquillo, María E. Gómez, "PS-Cache: An Energy-Efficient Cache Design for Chip Multiprocessors". Journal of Supercomputing (JSC), vol. 71 (1), pages 67--86, January 2015.

- Alberto Ros, Manuel E. Acacio, "DASC-DIR: a low-overhead coherence directory for many-core processors". Journal of Supercomputing (JSC), vol. 71 (3), pages 781--807, March 2015.
- Alberto Ros, Polychronis Xekalakis, Marcelo Cintra, Manuel E. Acacio, José M. García, "Adaptive Selection of Cache Indexing Bits for Removing Conflict Misses". IEEE Transactions on Computers (TC), vol. 64 (6), pages 1534--1547, June 2015.
- Joan J. Valls, Alberto Ros, Julio Sahuquillo, María E. Gómez, "PS Directory: A Scalable Multilevel Directory Cache for CMPs". Journal of Supercomputing (JSC), vol. 71 (8), pages 2847--2876, August 2015.
- Albert Esteve, Alberto Ros, María E. Gómez, Antonio Robles, José Duato, "Efficient TLB-Based Detection of Private Pages in Chip Multiprocessors". IEEE Transactions on Parallel and Distributed Systems (TPDS), vol. , 2015.
- Mahdad Davari, Alberto Ros, Erik Hagersten, Stefanos Kaxiras, "The Effects of Granularity and Adaptivity on Private/Shared Classification for Coherence". ACM Transactions on Architecture and Code Optimization (TACO), vol. 12 (3), pages 26:1--26:21, August 2015.

Book chapters:

- Alberto Ros, Manuel E. Acacio and José M. García, “Cache Coherence Protocols for Many-Core CMPs”. Parallel and Distributed Computing, January 2010 2009.

Books:

- Alberto Ros, "Parallel and Distributing Computing". IN-TECH, January 2010. (Editor)
- Alberto Ros, "Efficient and Scalable Cache Coherence for Chip Multiprocessors: Novel Proposals for Managing Cache Coherence in Future Many-Core Chip Multiprocessors". LAP Lambert Academic Publishing, February 2010.

PROJECTS

Participation in 3 regional projects, 6 national projects, and 4 European projects, and IP of one regional project. In the following, there is a list of the most relevant projects (including their duration), which show increasing responsibilities:

2014 – 2016	“Mejora del rendimiento y eficiencia de los multiprocesadores en un único chip basada en la naturaleza de los datos accedidos por aplicaciones”. Young Leaders in Research.Regional (Murcia, Spain). Role: IP of the project.
2013 – 2014	“VIPS”. VINN-Verifiering. National (Sweden). Role: Further develop and commercialize the VIPS family of protocols.
2013 – 2015	“Mejora de las arquitecturas de servidores, aplicaciones y servicios”. National (Spain). Role: Task leader in the track on cache coherence protocols.
2011 – 2014	“Low-power GPU (LPGPU)”.

European.
Role: Researcher in the design virtual cache coherence techniques.

2010 – 2012 "A Highly Efficient Adaptive multi-Processor framework (HEAP)".
European.
Role: Researcher in the design of VIPS cache coherence protocol.

2010 – 2012 "Arquitecturas de servidores, aplicaciones y servicios".
National (Spain).
Role: Researcher in the track on cache coherence protocols.

2010 – 2012 "Arquitecturas de servidores, aplicaciones y servicios".
National (Spain).
Role: Researcher in the track on cache coherence protocols.

2008 – 2017 "Uppsala Programing for Multicore Research Center (UPMARC)".
National (Sweden).
Role: Postdoc and visiting researcher working on cache coherence protocols.

2006 – 2009 "Mejora de las Prestaciones, Servicios y Aplicaciones Ofrecidas por Arquitecturas Cluster de Altas Prestaciones".
National (Spain).
Role: Researcher in the track on cache coherence protocols.

2006 – 2011 "Arquitecturas Fiables y de Altas Prestaciones para Centros de Proceso de Datos y Servidores de Internet".
Consolider project. National (Spain).
Role: Researcher in the track on cache coherence protocols.

PARTICIPATION IN PROGRAM COMMITTEE AND REVIEWER

- Program committee of IADIS'09 – '14, ICPP'13, and OMHI'13.
- External program committee of PACT'14, ISCA'15.
- Reviewer in journals: IET Computers & Digital Techniques, Computer Architecture Letters, Computing, The Computer Journal, Concurrency and Computation: Practice and Experience, Journal of Computer Science and Technology, Journal of Parallel and Distributed Computing, Journal of Systems Architecture, IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems and IEEE Transactions on Very Large Scale Integration Systems.

TEACHING

2010 – 2015 Lecturer, Computer Science, Universidad de Murcia, Spain B.Sc. on Computer Science: Estructura y Tecnología de Computadores –Computer Architecture I– (2012/2013, 2013/2014, 2014/2015), Arquitectura e Ingeniería de Computadores – Computer Architecture III– (2010/2011, 2011/2012), Redes de Computadores – Computer Networks I– (2011/2012, 2012/2013, 2013/2014, 2014/2015), Tecnologías

Específicas de la Ingeniería Informática –Specific Technologies in Computer Engineering– (2011/2012, 2012/2013, 2013/2014, 2014/2015). M.Sc. on New Technologies in Computer Science: Integration of Networks (2011/2012, 2012/2013, 2013/2014).

2006 – 2009 Teaching assistant, Computer Science, Universidad de Murcia, Spain B.Sc. on Computer Science: Arquitectura e Ingeniería de Computadores –Computer Architecture III– (2006/2007, 2007/2008, 2008/2009), Diseño de Arquitecturas de Alto Rendimiento –Design of High-Performance Architectures– (2006/2007, 2007/2008, 2008/2009).

OTHER ACTIVITIES

- Twice finalist on the South Western European Regional of the ACM International Programming Contest (SWERC 2003 and 2004).
- Assistance to the "Second International Summer School on Advanced Architecture and Compilation for Embedded Systems (ACACES'06)". July 23-29, 2006.
- Twice coach of a team for the South Western European Regional of the ACM International Programming Contest (SWERC 2009 and 2010).
