RACER: TSO CONSISTENCY VIA RACE DETECTION

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Outline

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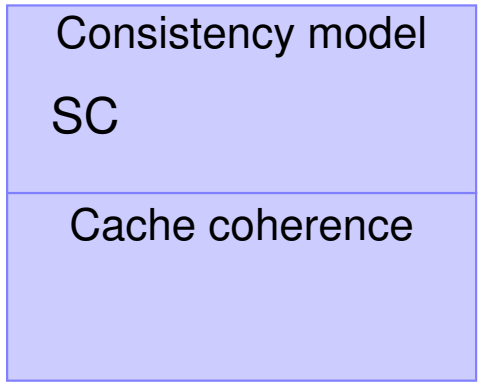
Cache coherence (SC)

- Cache coherence problem studied for several decades
- Cache coherence serves as a black box to support strict consistency models: e.g., Sequential Consistency (SC)



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  - Single-writer-multiple-readers (SWMR) invariant
  - Invalidation/update of the copies on every write
  - Large amount of traffic $\Rightarrow$ increases energy consumption

Consistency model
SC
Cache coherence
SWMR $\Rightarrow$ Energy

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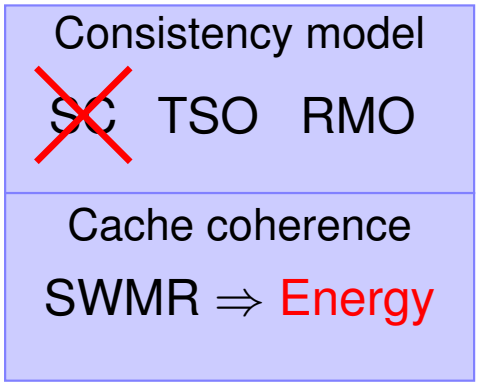
Most processors offer consistency models weaker than SC



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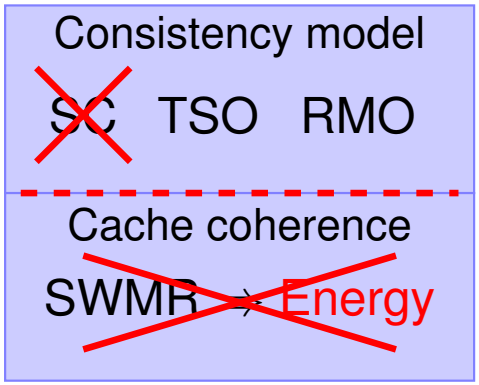
Observation 1

Most processors offer consistency models weaker than SC

- Why implement protocols that provide more functionality than necessary?
- Protocol as a black box?
  - Break the layer between the consistency model and the coherence protocol!



CACHE COHERENCE (SC-FOR-DRF)

- Simple cache coherence: VIPS-M *[Ros & Kaxiras, PACT'12]*
  - Strictly request-response ⇒ Simple
  - Allows virtual caches without reverse translation ⇒ Efficient
  - Coherence distributed across cores ⇒ Scalable
  - No directory ⇒ Simple and scalable

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Example of DRF code

`X = 1;`	`WAIT(cond);`
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  - ⇒ Write-through dirty blocks

EXAMPLE OF DRF CODE

SD

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EXAMPLE OF DRF CODE

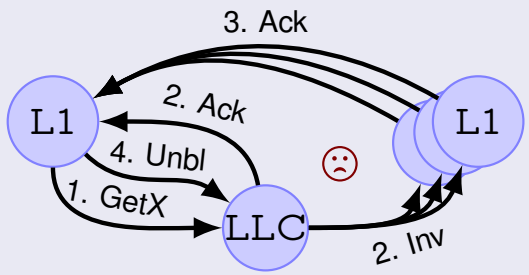
```
SD   X = 1;              |  WAIT(cond);   SI
     SIGNAL(cond);       |  $r1 = X;
```

OBSERVATION 2

SI & SD are conservatively performed because of static synchronization even if there is no actual value propagation between cores

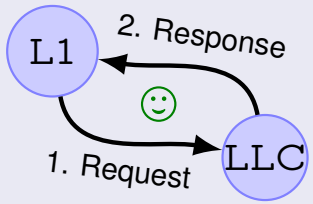
SC VERSUS SC-FOR-DRF COHERENCE

SC



☺ Works for all codes

SC-FOR-DRF



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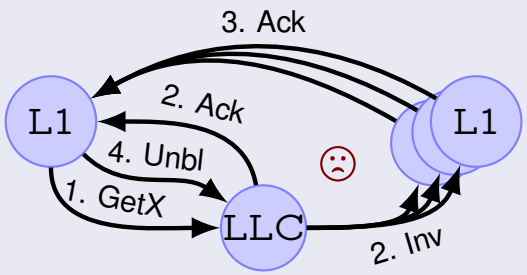
SC versus SC-for-DRF coherence

SC



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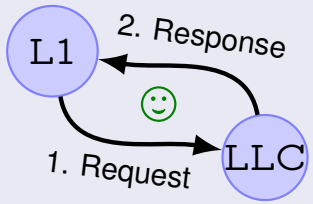

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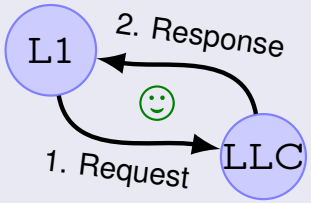
Racer (Total-Store-Order – TSO)



☺ Works for all (TSO) codes

First efficient, request-response protocol for all codes

TSO MEMORY CONSISTENCY

TSO RULES

- load→load
- store→store
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```
/* Initially X, Y = 0 */

X = 1;          |  $r1 = Y;
Y = 1;          |  $r2 = X;

/* $r1 == 1 and $r2 == 0 not allowed */
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POSSIBLE EXECUTION

```
Y = 1;          |
X = 1;          |
                |  $r1 = Y;
                |  $r2 = X;

/* (1, 1) allowed */
```

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OBSERVATION 3

Memory operations can be safely reordered as long as they are not observed by other cores

- Is it always necessary to ensure these rules?

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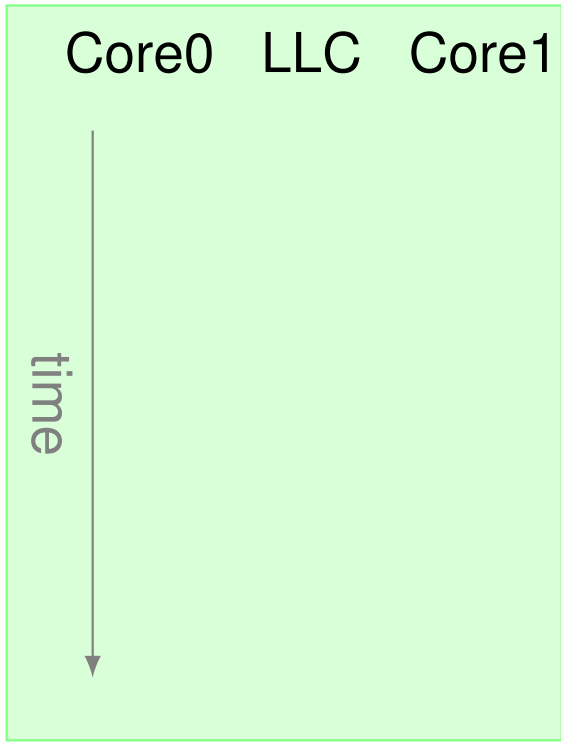

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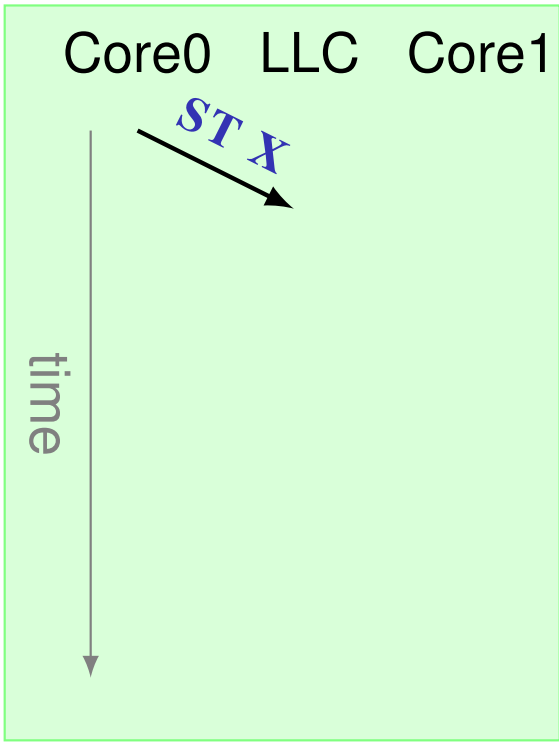

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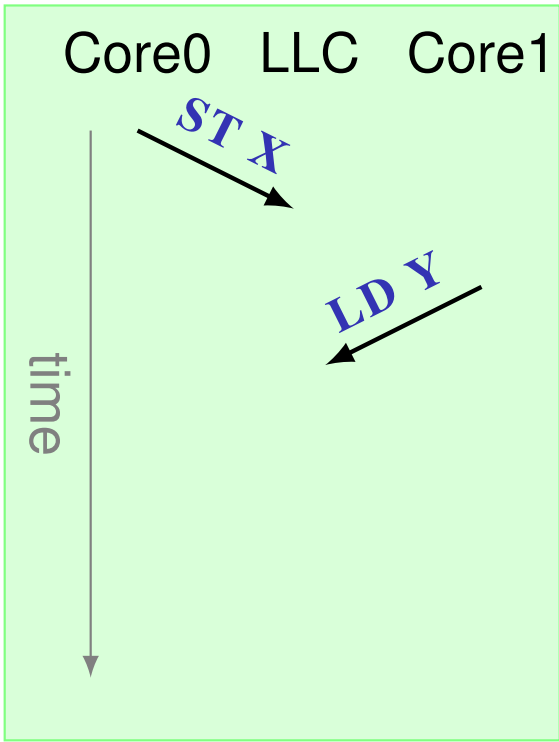

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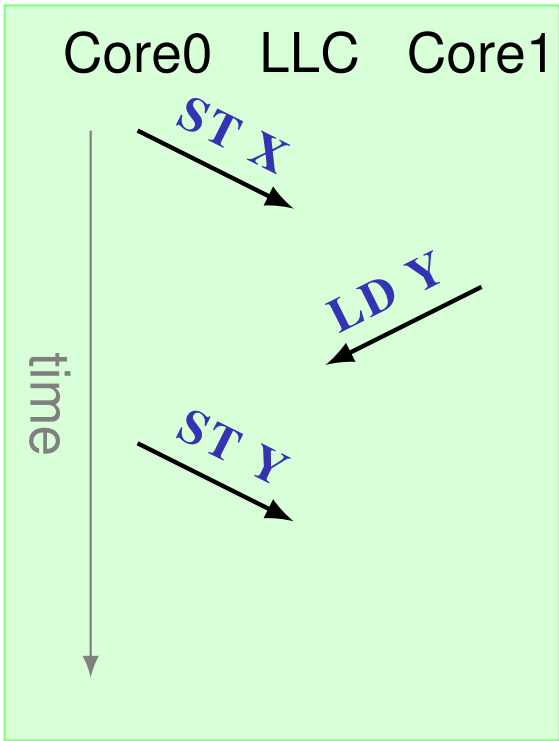

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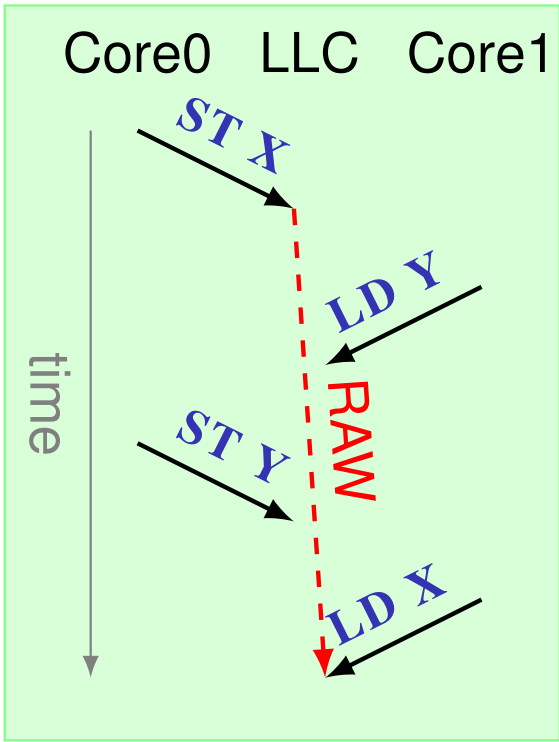

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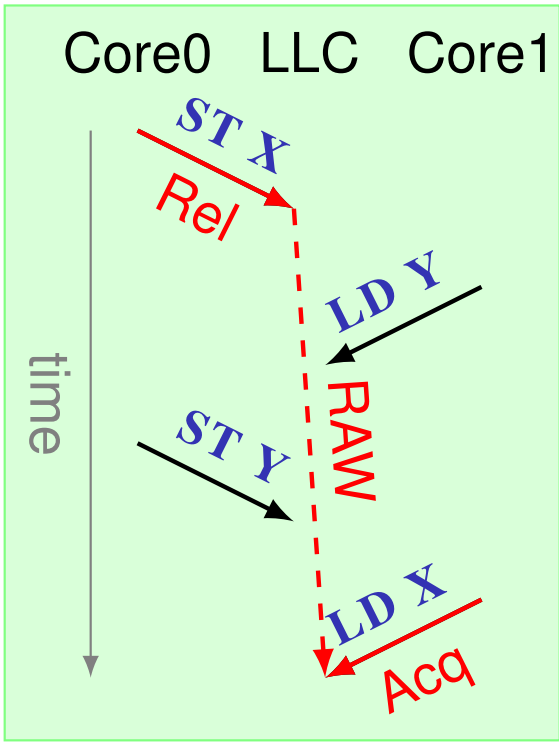

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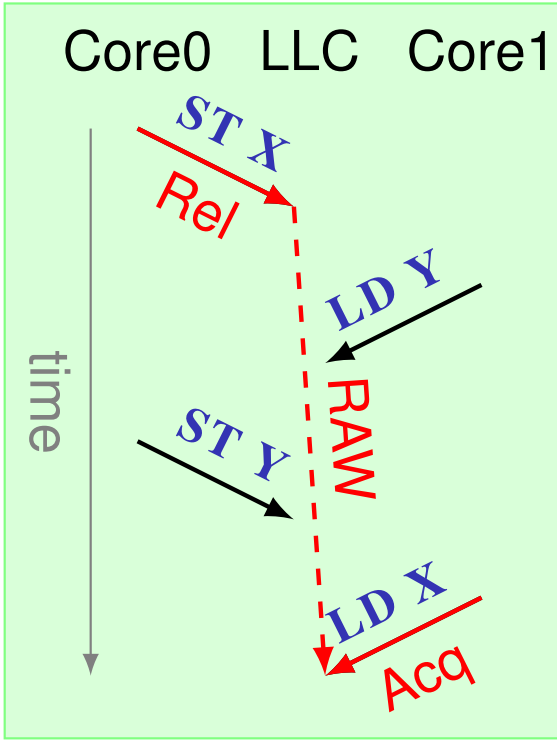
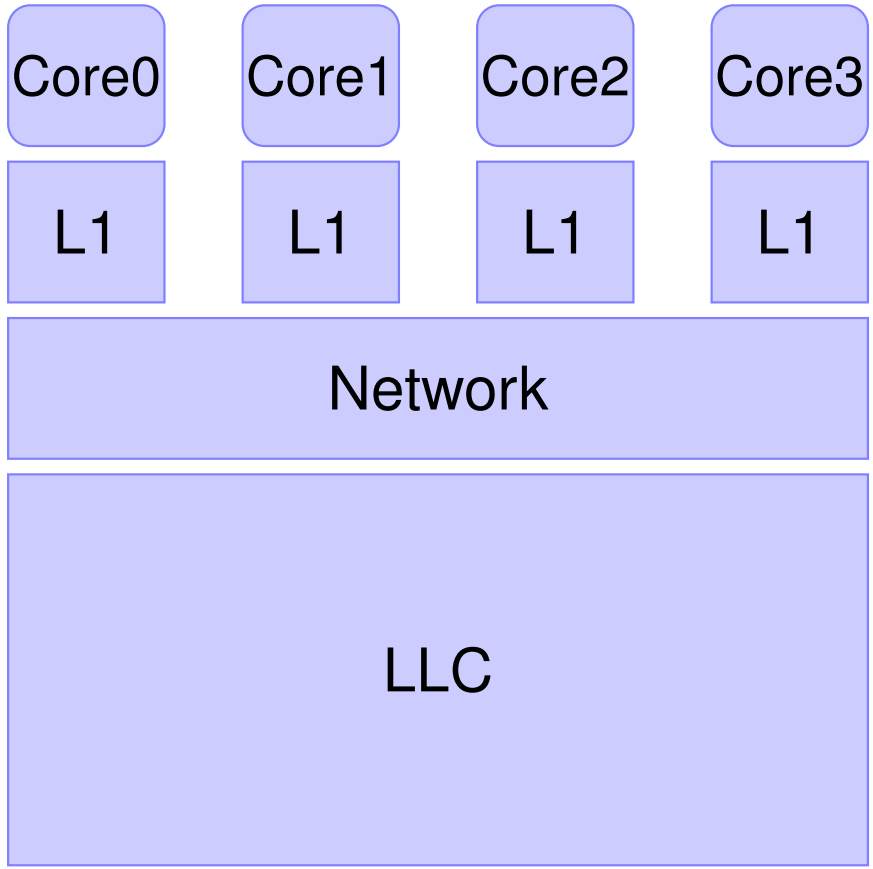
- Consistency only enforced for shared data *[Singh et al. ISCA'12]*



BASIC OPERATION



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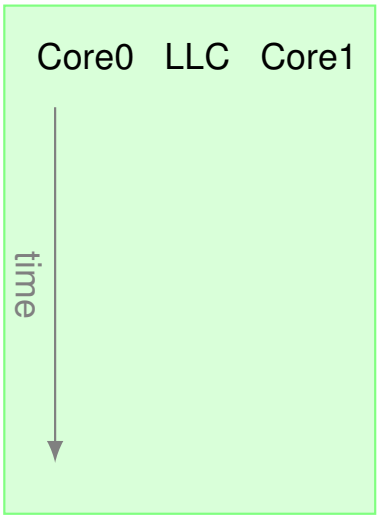
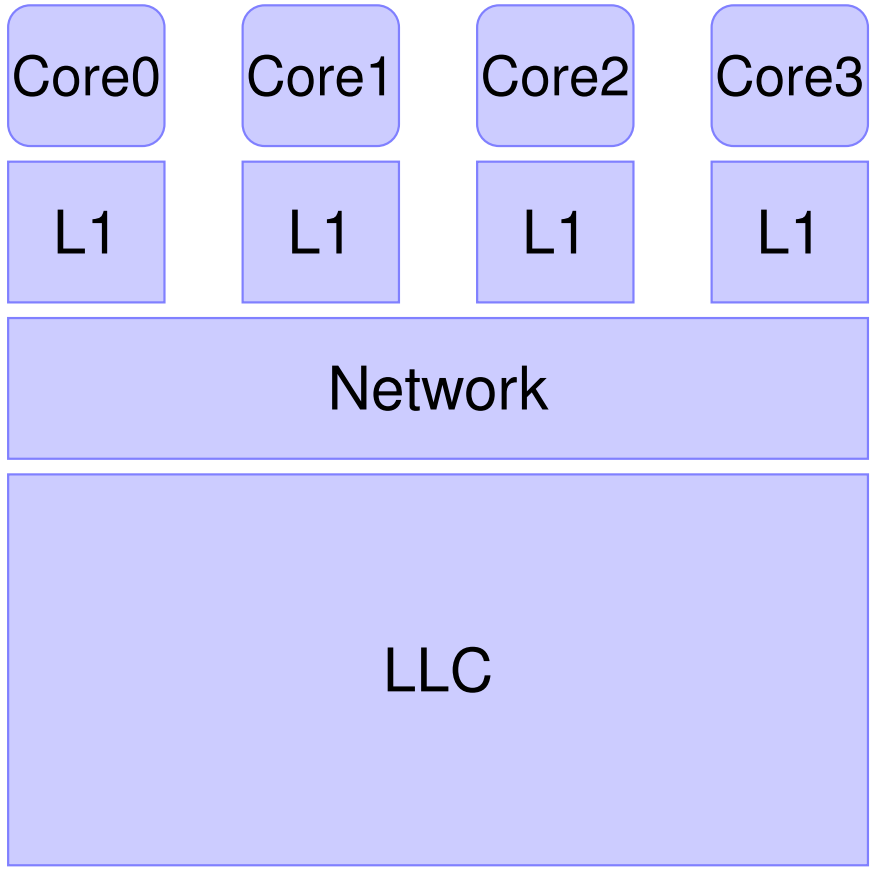


One bloom filter per core

RAWR DETECTOR

Core	Bloom filter
0	
1	
2	
3	



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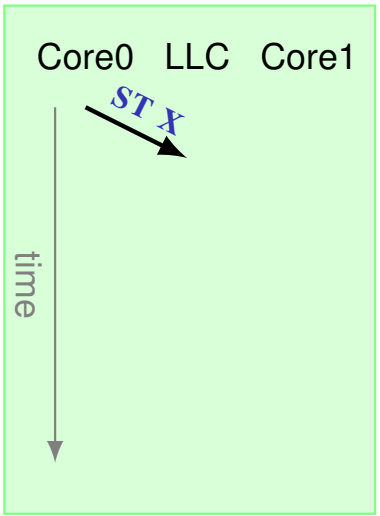
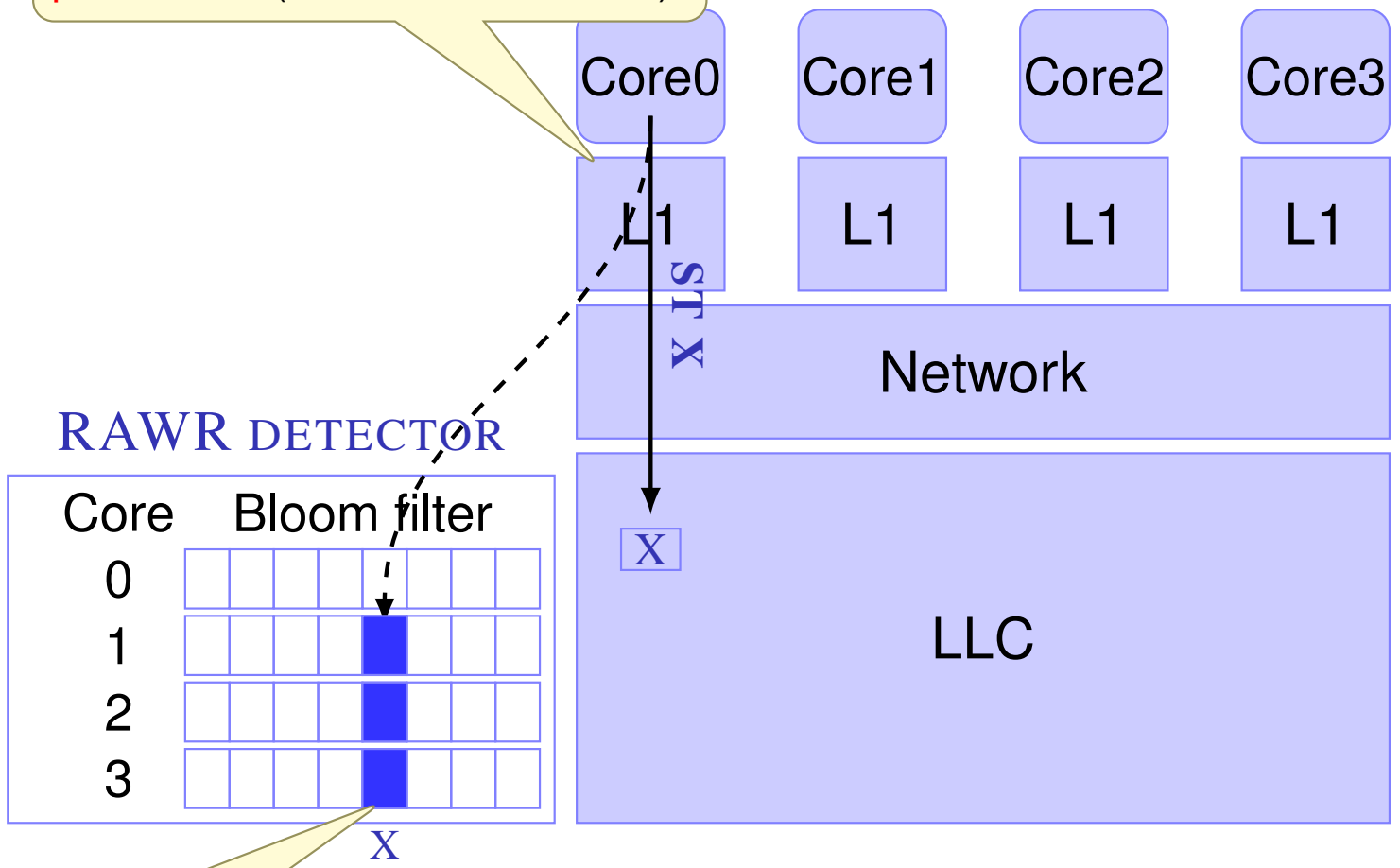
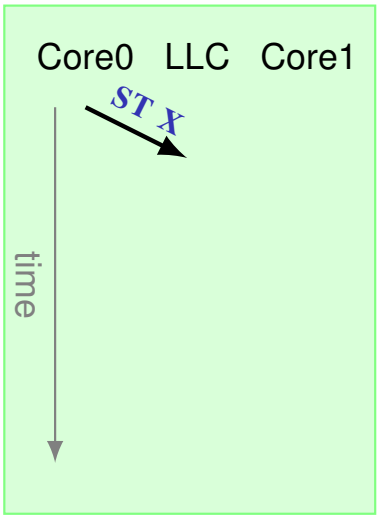


Stores do not require write permission (no SWMR invariant)

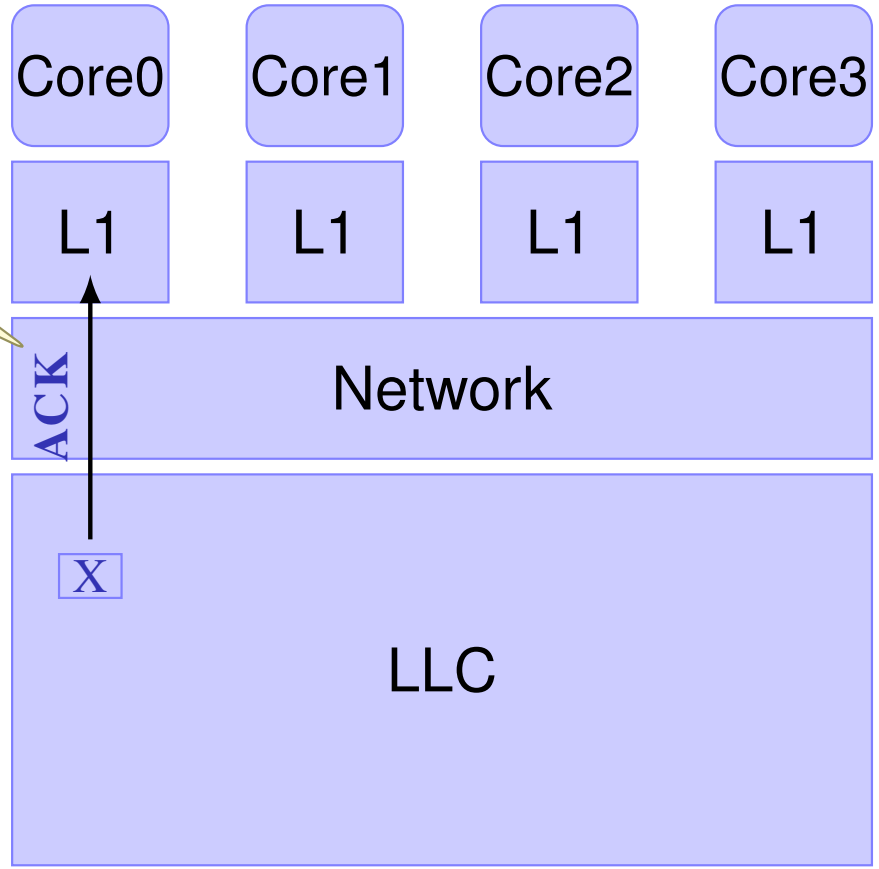


Cores 1, 2, and 3 have not seen the write to x

BASIC OPERATION



ACK to guarantee order of store operations



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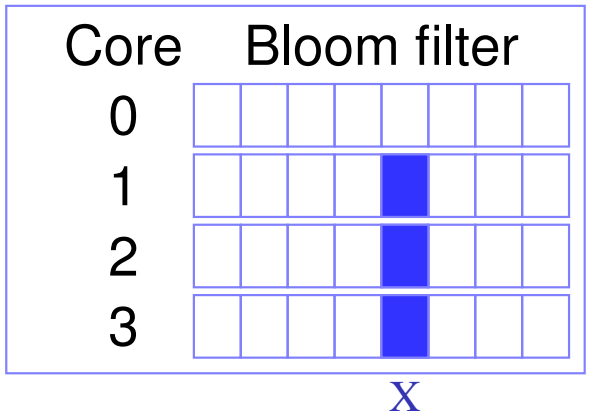

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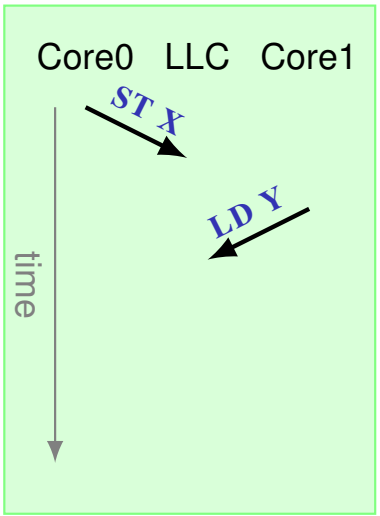

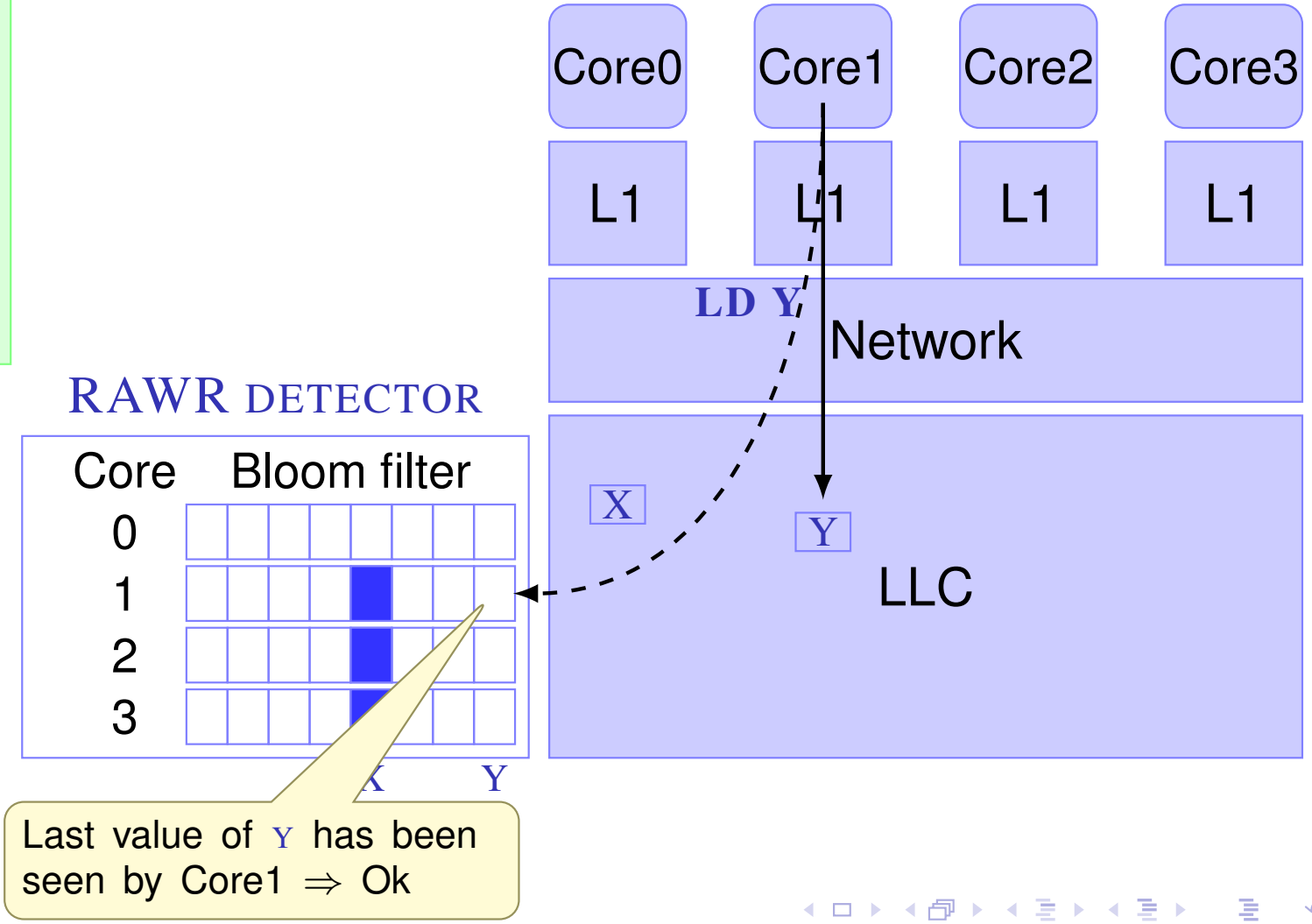

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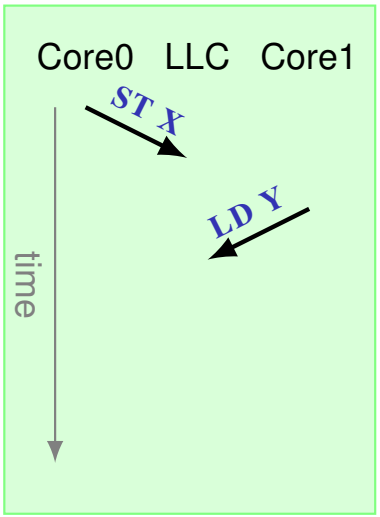

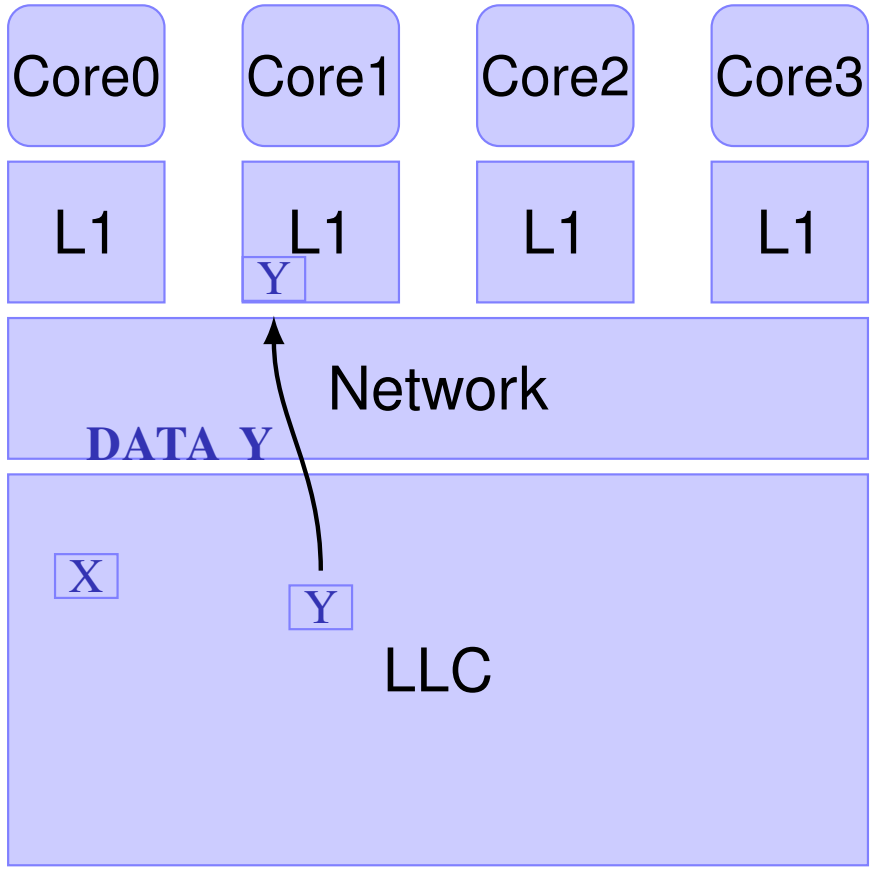

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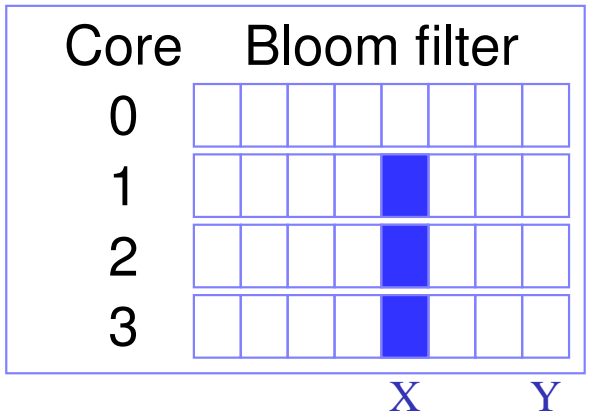

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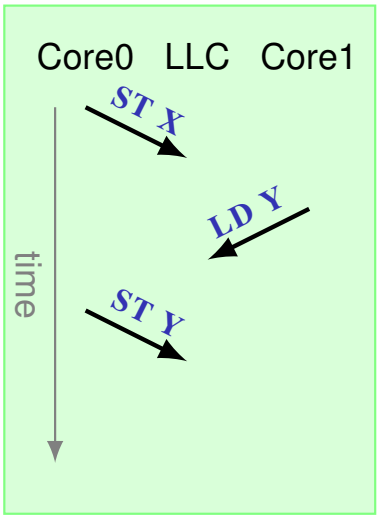

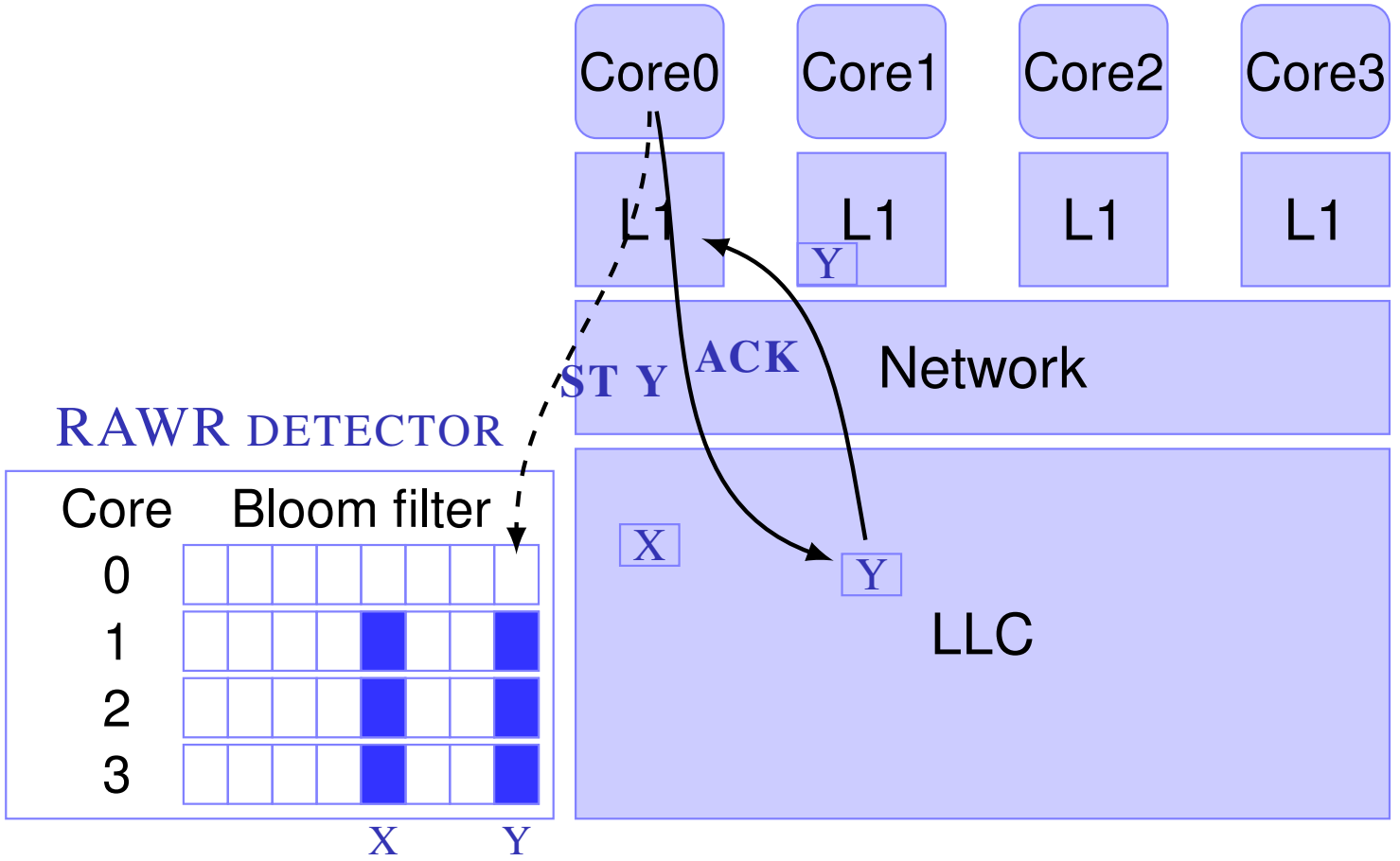

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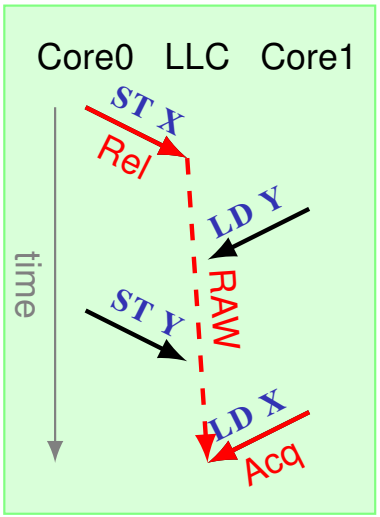

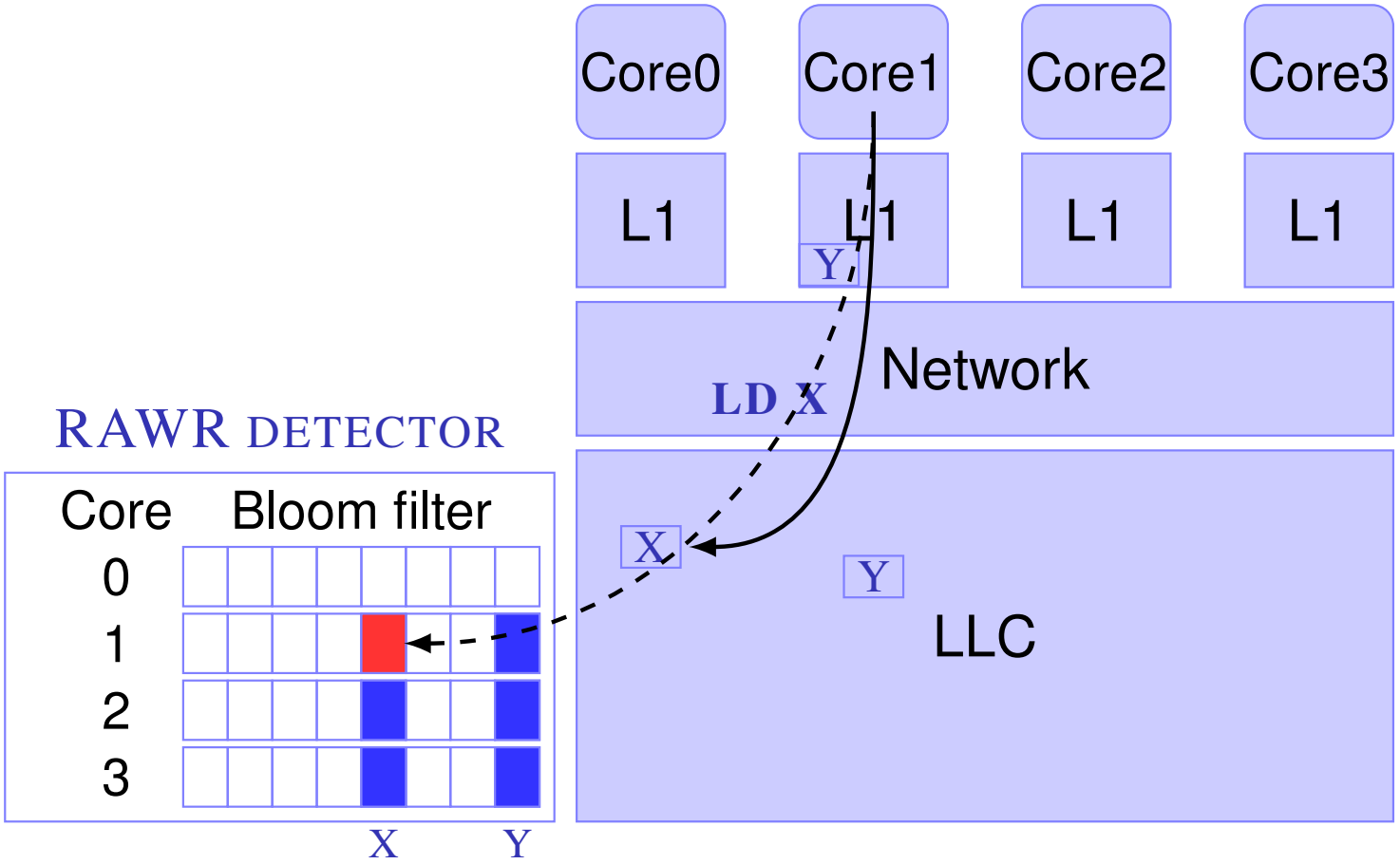

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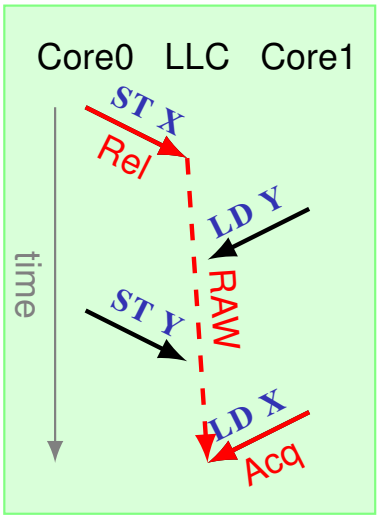

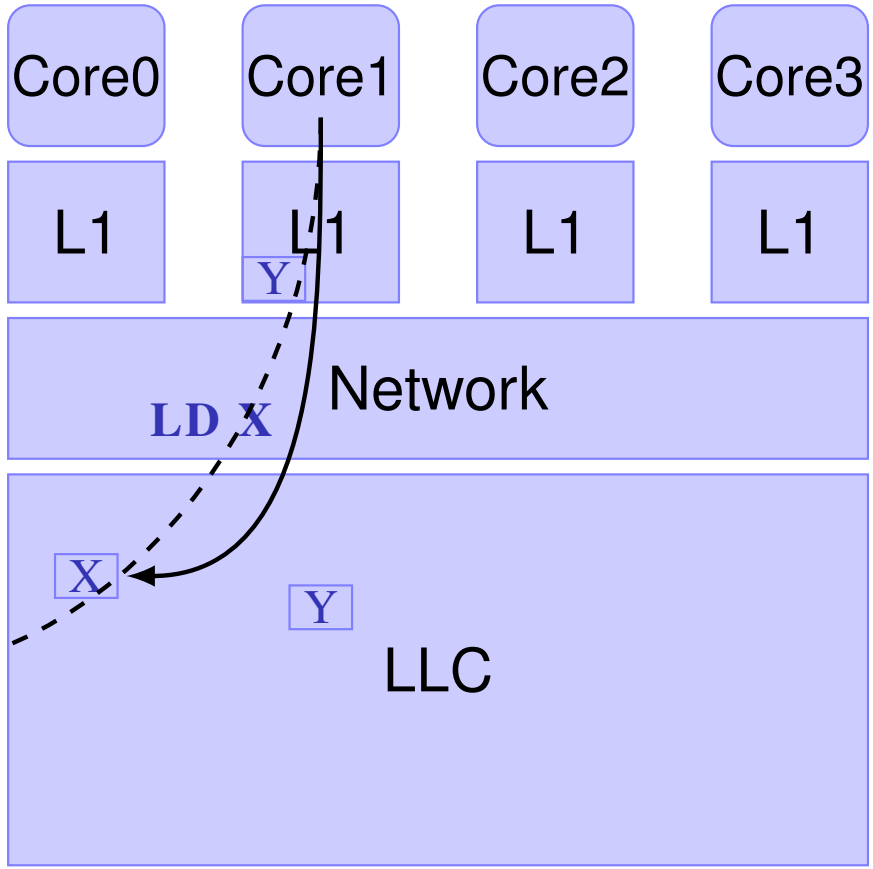

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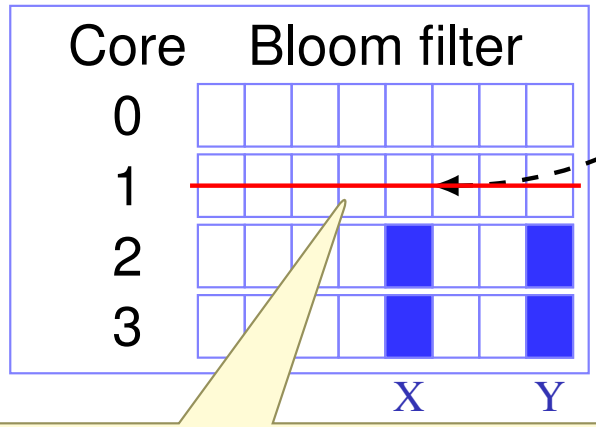
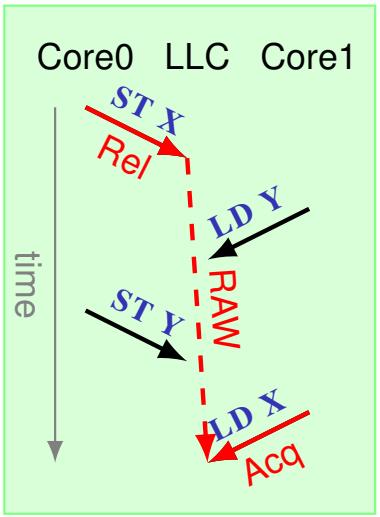


Clean Core1 bloom filter.
Filters are naturally cleared when detecting races!

BASIC OPERATION



SELF-INVALIDATE (shared)
Core1 cache content

Core0 Core1 Core2 Core3

L1 L1 L1 L1

X X

Network

DATA X + SI

X

Y

LLC

RAWR DETECTOR

Core	Bloom filter
0	
1	
2	X Y
3	X Y

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1. Write-through ⇒ Traffic, energy
   - Solution: Coalesce, but keep TSO order
2. L1 hits cannot detect races ⇒ Starvation
   - Solution: Check-for-race, but efficient

Coalescing and TSO order

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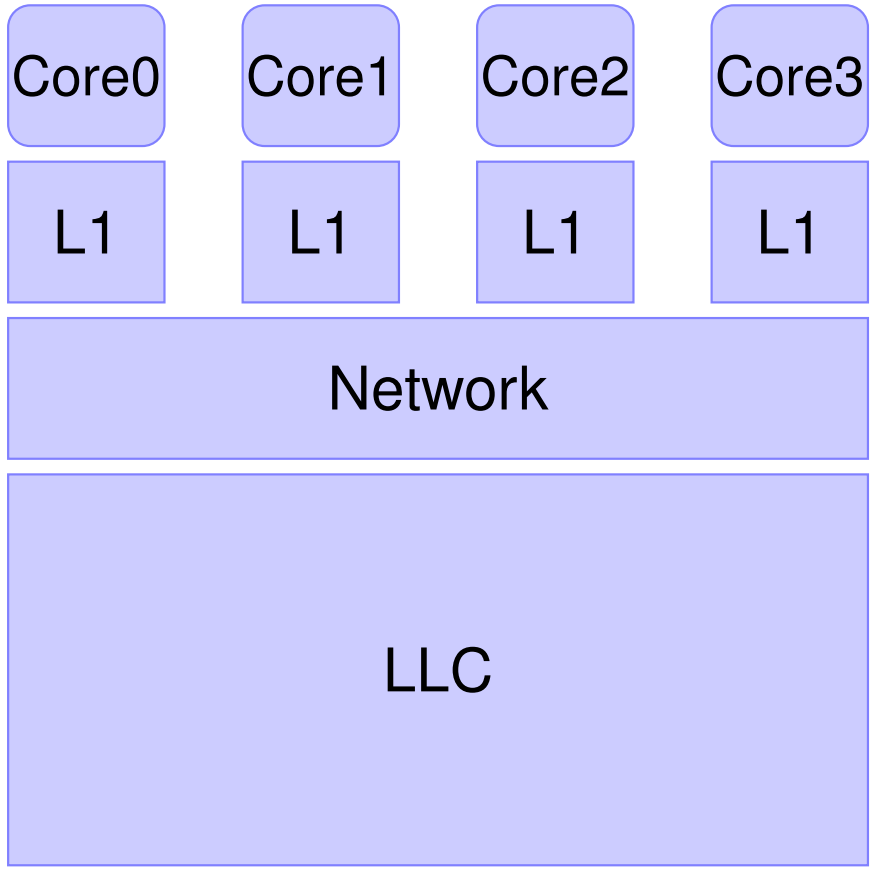
  - Write coalescing violates the `store`→`store` order

COALESCING AND TSO ORDER

- How to coalesce without violating TSO order?
  - Write coalescing violates the `store`→`store` order
- Only a problem if someone sees the reordering (Obs.3)
- Solution: COLLAPSED ORDER
  - ⇒ Allows to coalesce non-consecutive stores
  - ⇒ By not allowing observing reorderings

Coalescing and collapsed order



RAWR detector

Core	Bloom filter
0	
1	
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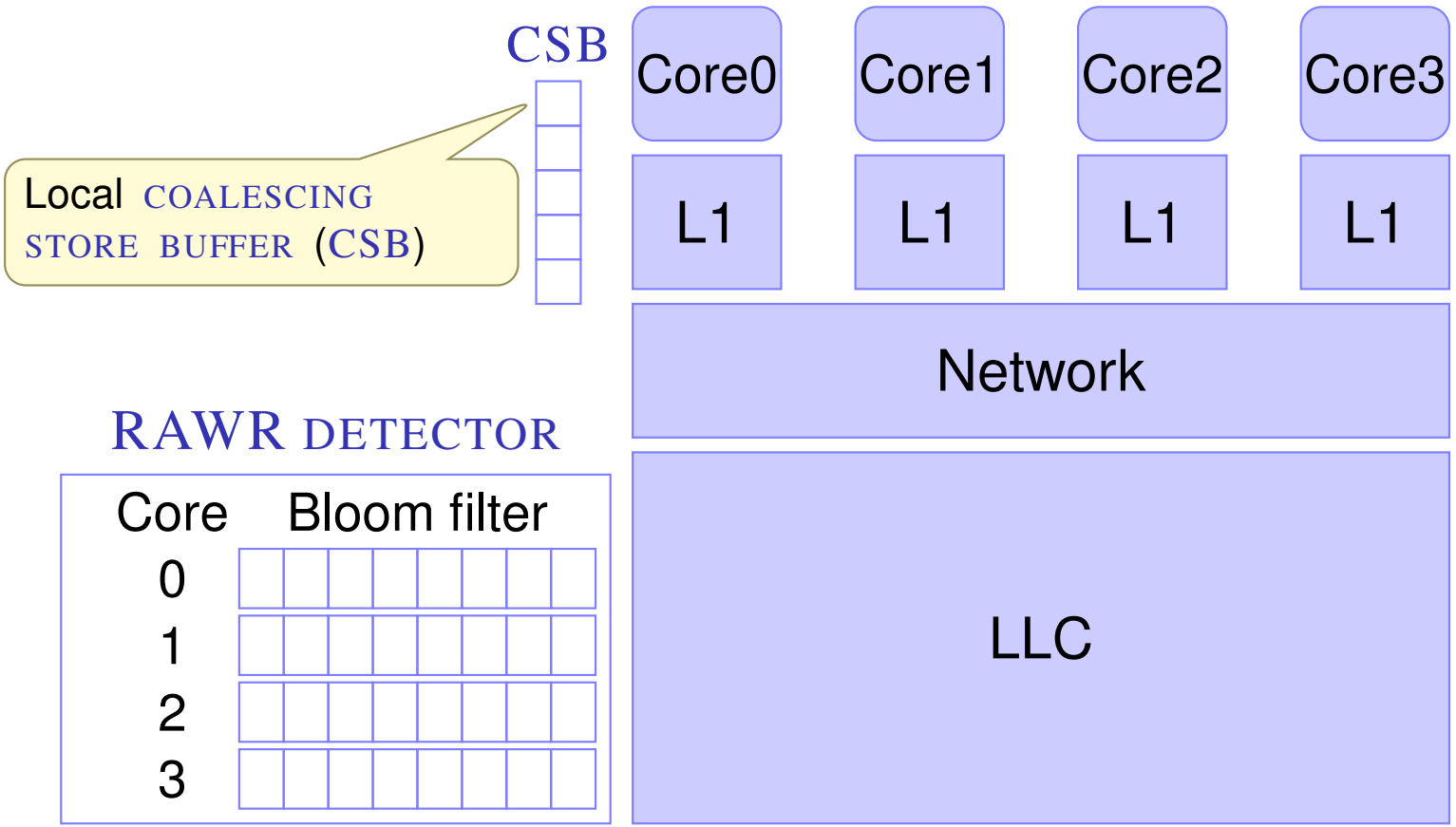
3	

COALESCING AND COLLAPSED ORDER



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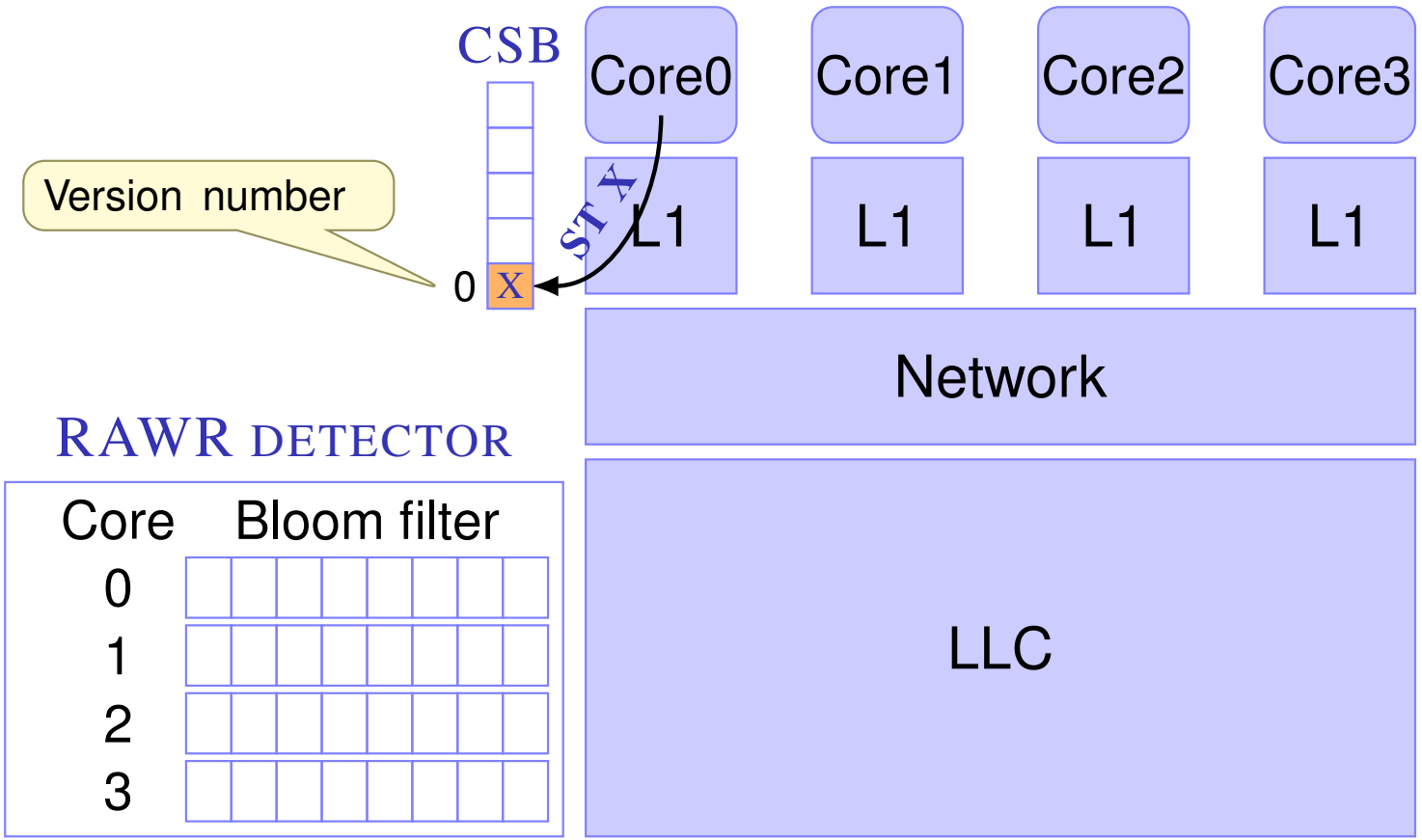
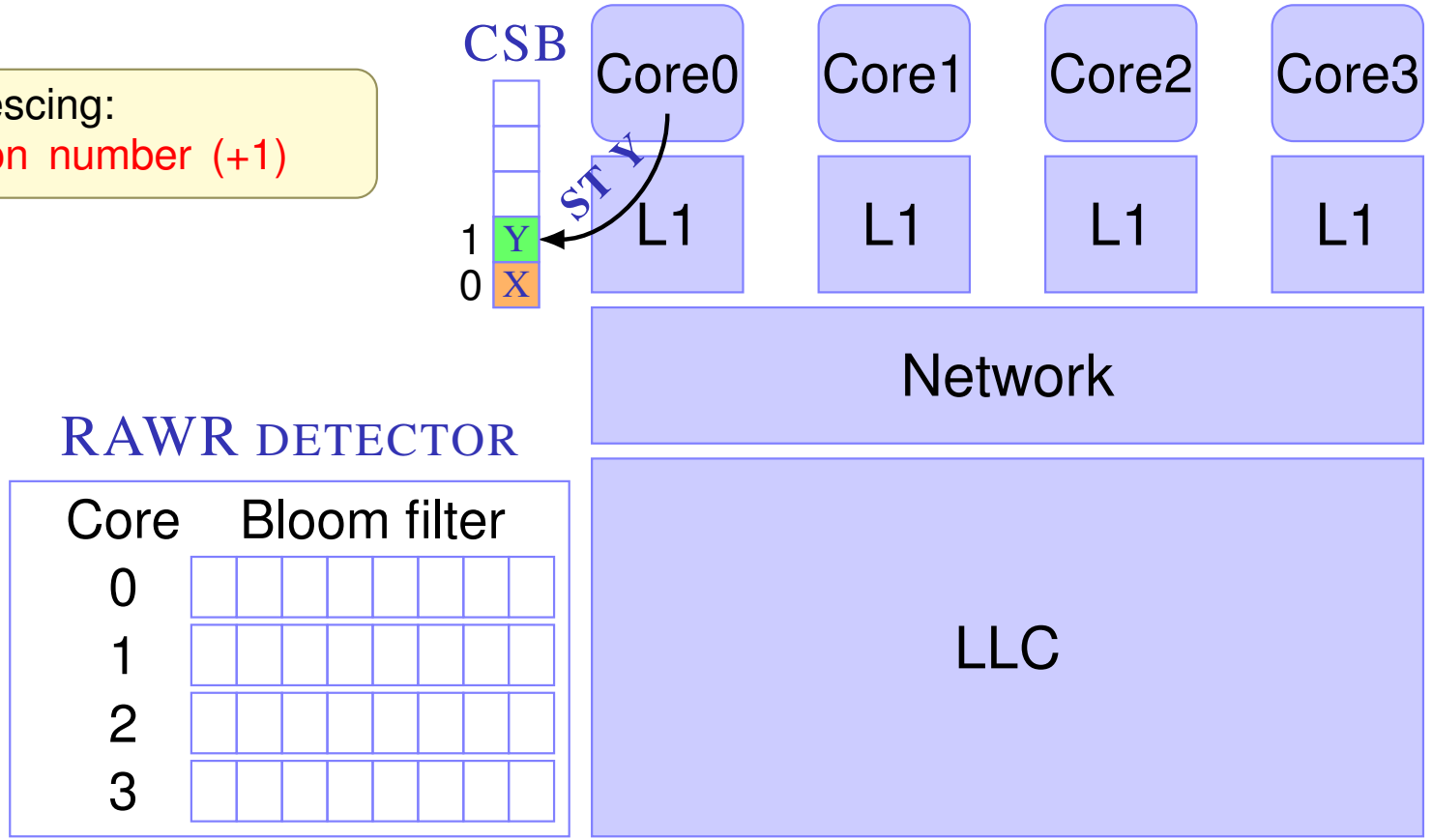


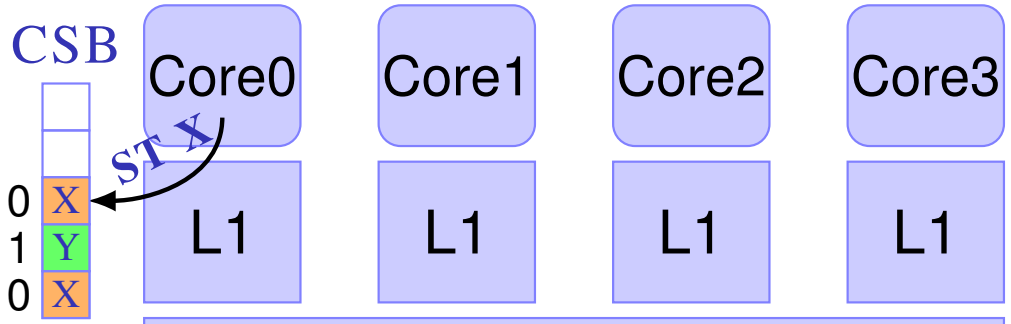
COALESCING AND COLLAPSED ORDER

No coalescing:
⇒ version number (+1)



COALESCING AND COLLAPSED ORDER

Coalescing:
$\Rightarrow$ all version numbers between coalescing writes the same



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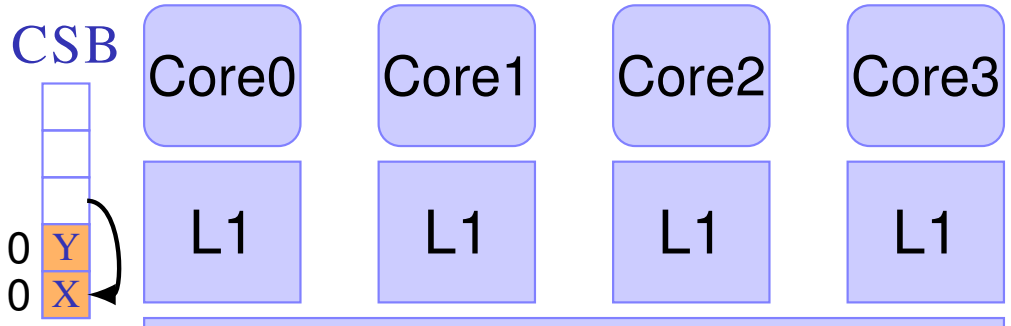

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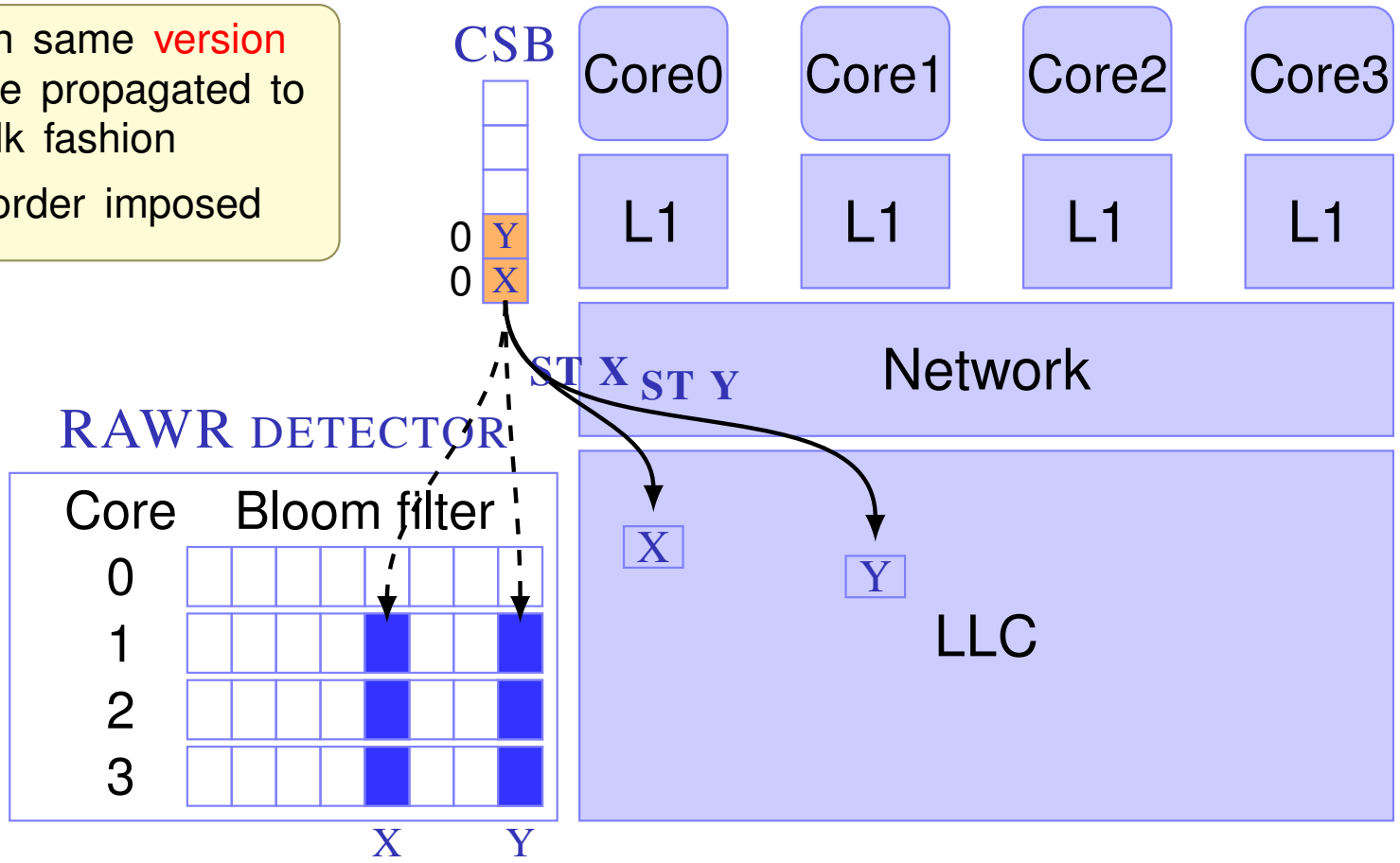
COALESCING AND COLLAPSED ORDER

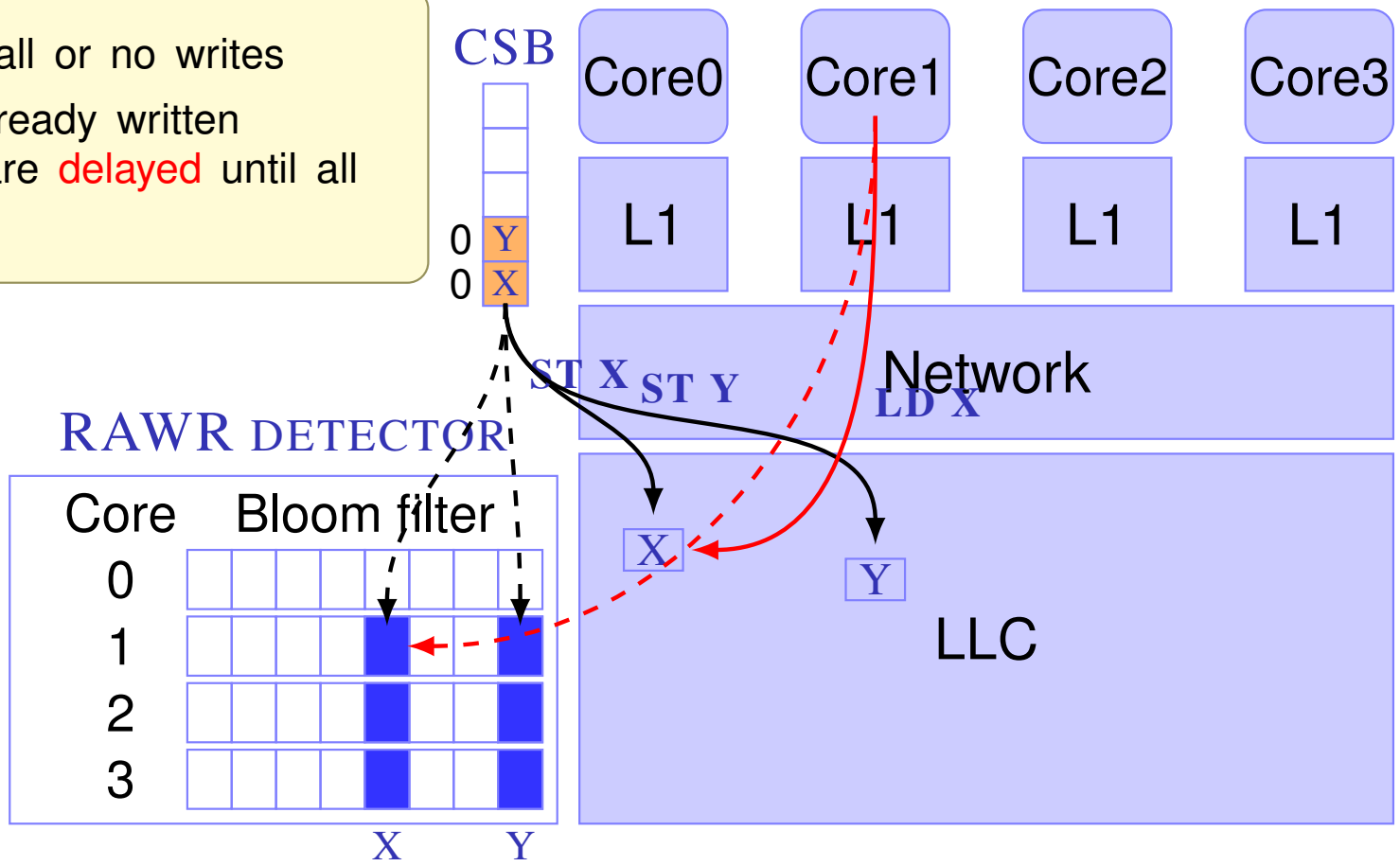
Writes with same version number are propagated to LLC in bulk fashion

$\Rightarrow$ No order imposed



Coalescing and collapsed order

- Reads see all or no writes
- Reads to already written addresses are delayed until all writes finish



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- Load→Store
  - SD performed after all previous loads are resolved

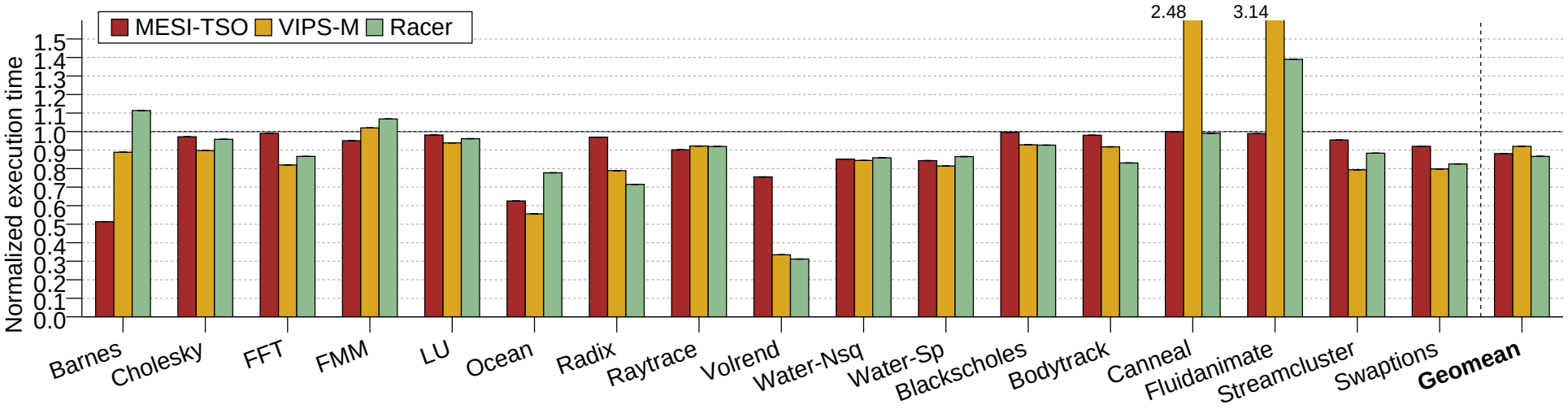
Outline

SIMULATION ENVIRONMENT

- 64-core tiled-CMP (GEMS simulator)
  - L1 (private): 32KB 4-way
  - LLC (shared): 256KB 16-way (per tile)
  - RAWR DETECTOR: 256-byte bloom filter
  - RACER overhead: ≈18KB per tile
- Benchmarks: Splash-3 and Parsec-2.1
- Protocols evaluated:
  - MESI: Directory-based SC protocol
  - MESI-TSO: Directory-based TSO protocol
  - VIPS-M: SC-for-DRF protocol
  - RACER: TSO protocol

EXECUTION TIME

- Normalized to MESI



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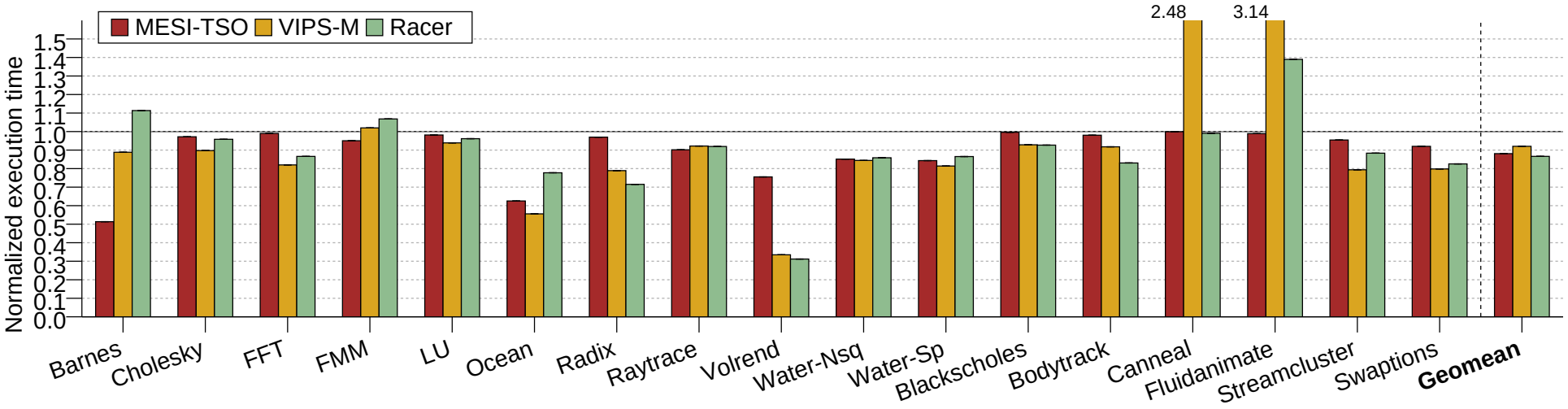

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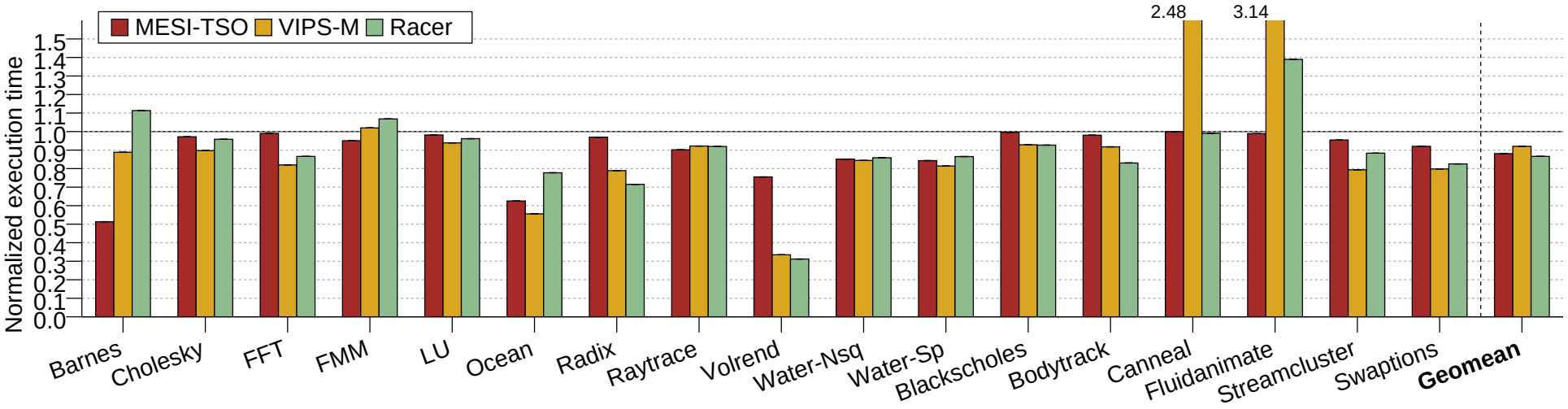
- RACER ≈ non-scalable MESI-TSO
- RACER: better performance than VIPS-M, while providing stronger consistency, but only when needed at run time



ENERGY CONSUMPTION

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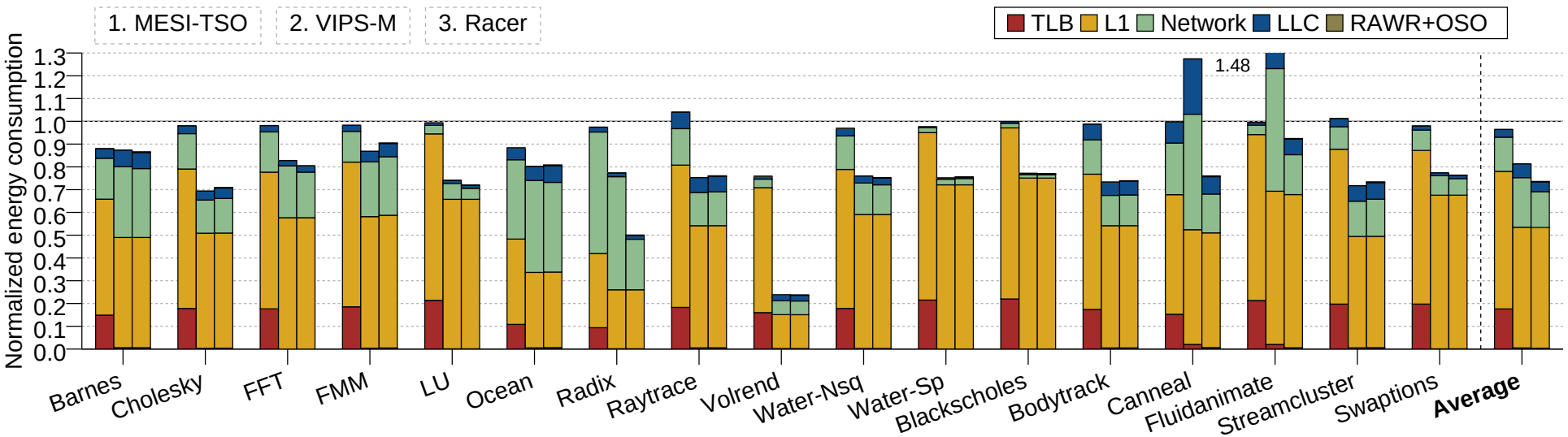

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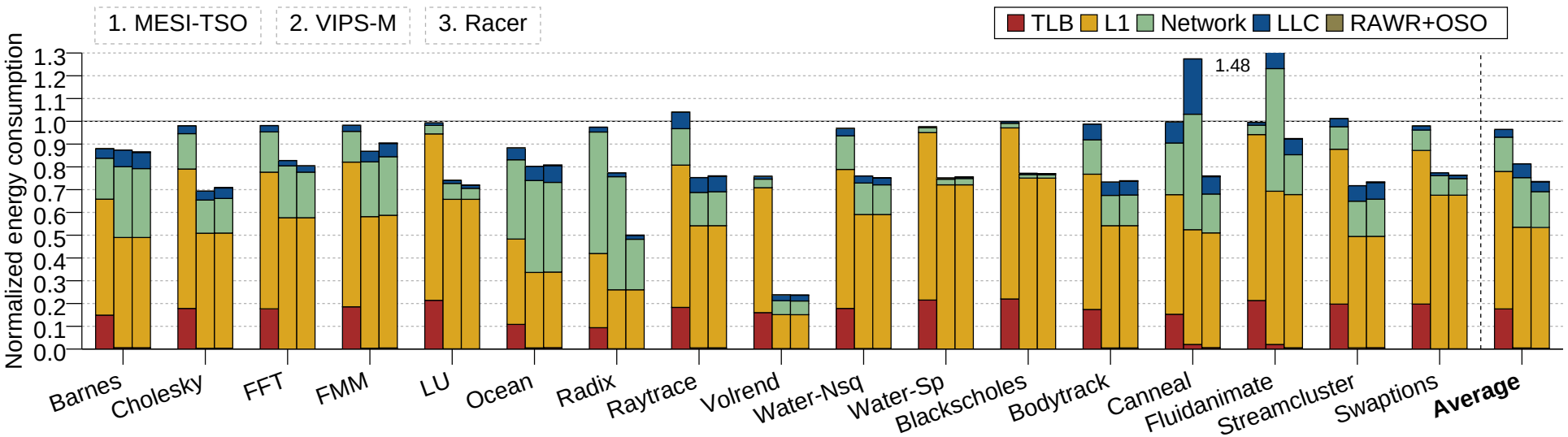

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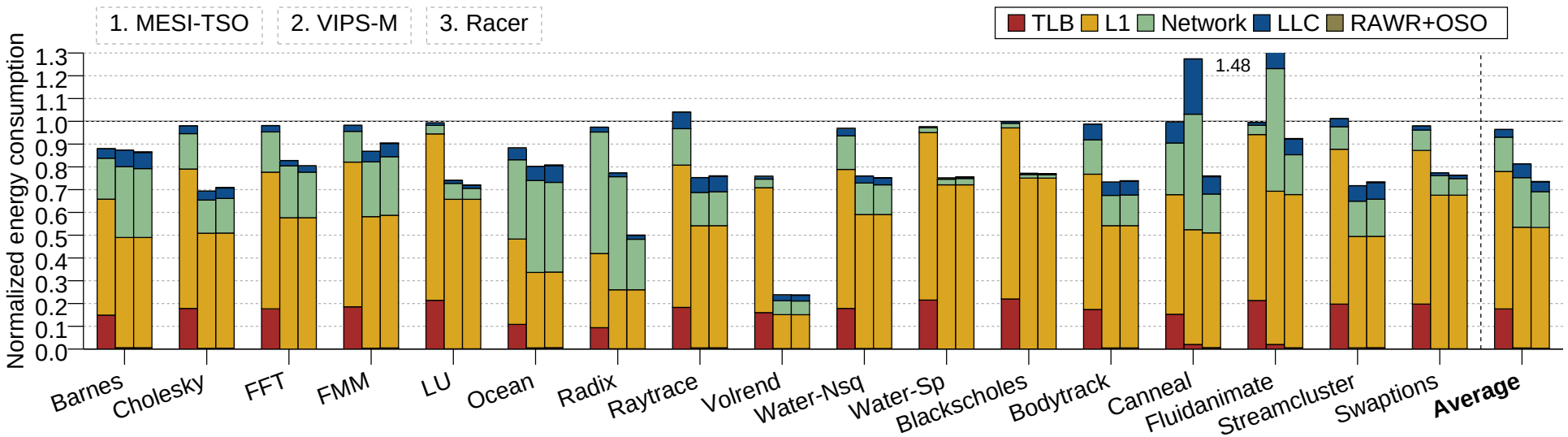

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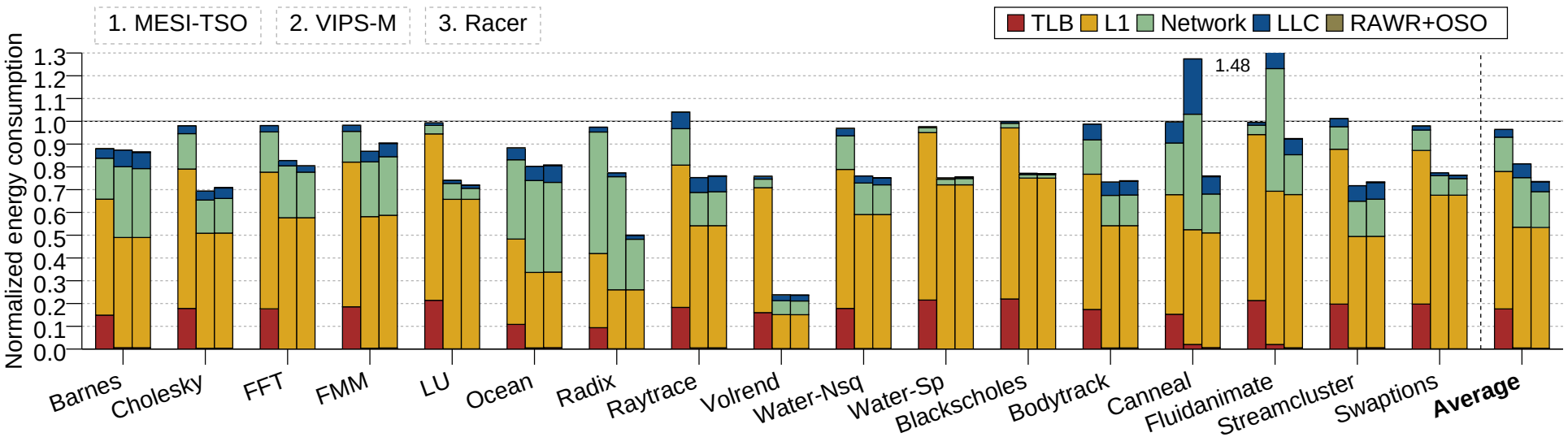
  - LLC and network consumption of MESI-TSO (runtime synchronization)



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- More in the paper
  - ⇒ Implementation of a distributed RAWR
  - ⇒ Implementation for OoO cores with speculation

RACER: TSO CONSISTENCY VIA RACE DETECTION

Alberto Ros[1] Stefanos Kaxiras[2]

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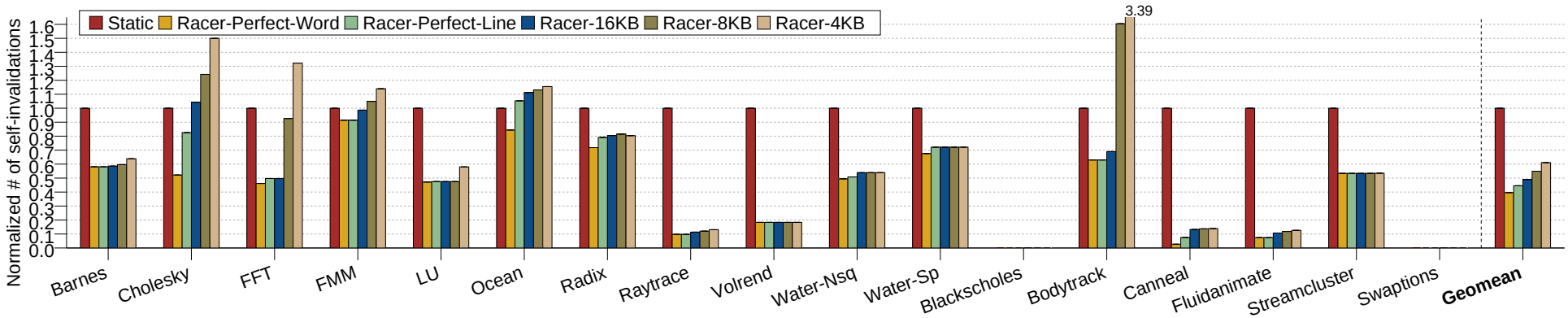
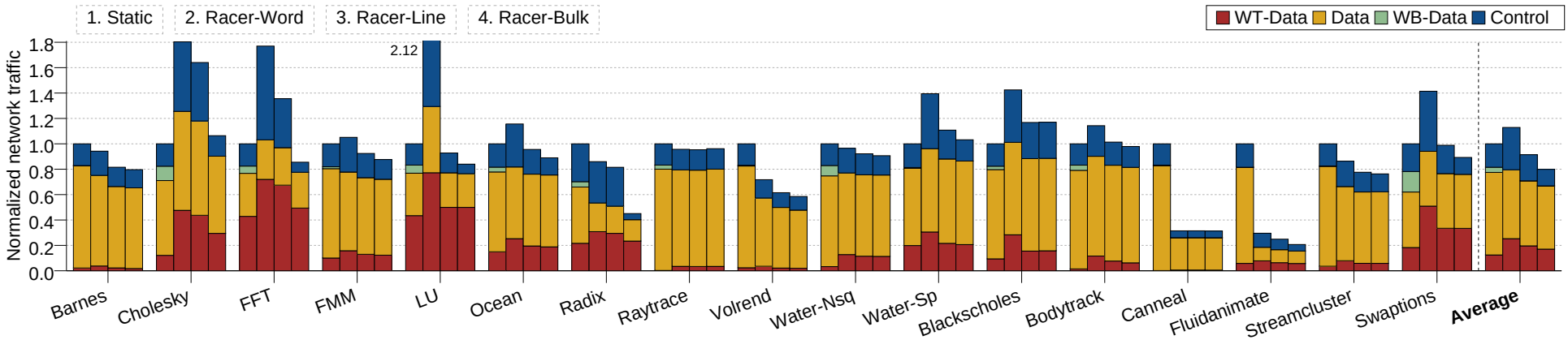
stefanos.kaxiras@it.uu.se

Nov 28th, 2016

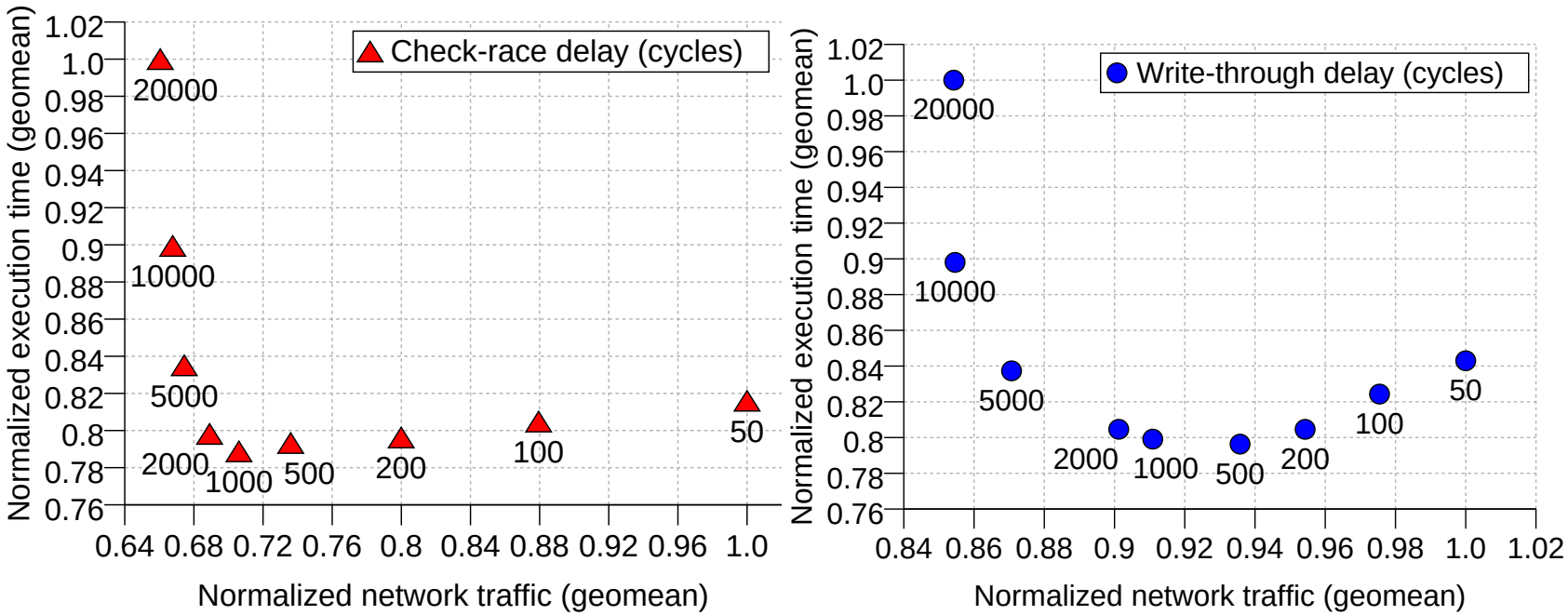
SELF-INVALIDATION



NETWORK TRAFFIC



SENSITIVITY



Protocol weaknesses and related work

Protocol	Strength	DRF	Dir	Time-stamps	Broad-cast	Indirection	Slow release

PROTOCOL WEAKNESSES AND RELATED WORK

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TSO-CC [HPCA'14]	TSO	—	—	✓	✓	✓	✓
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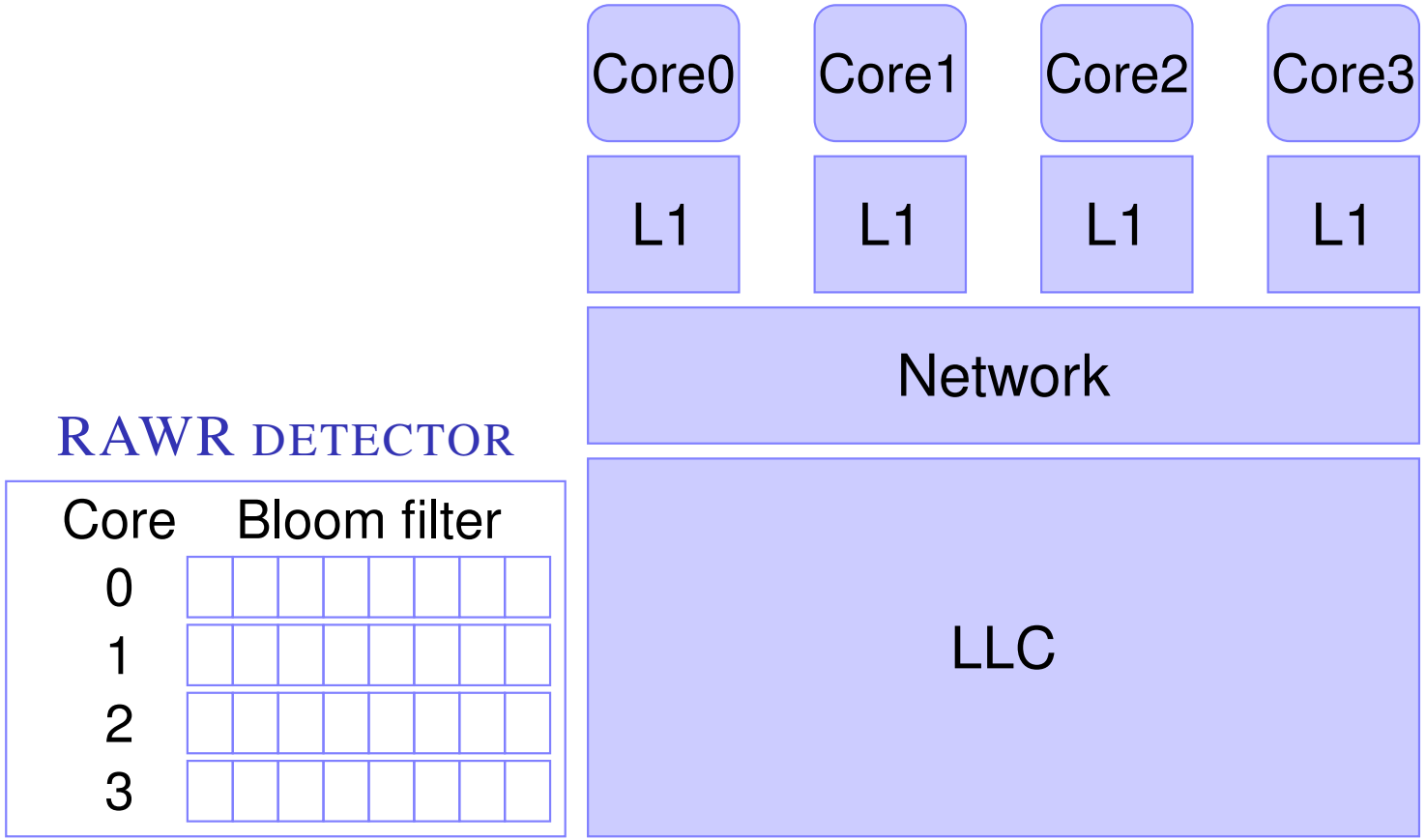
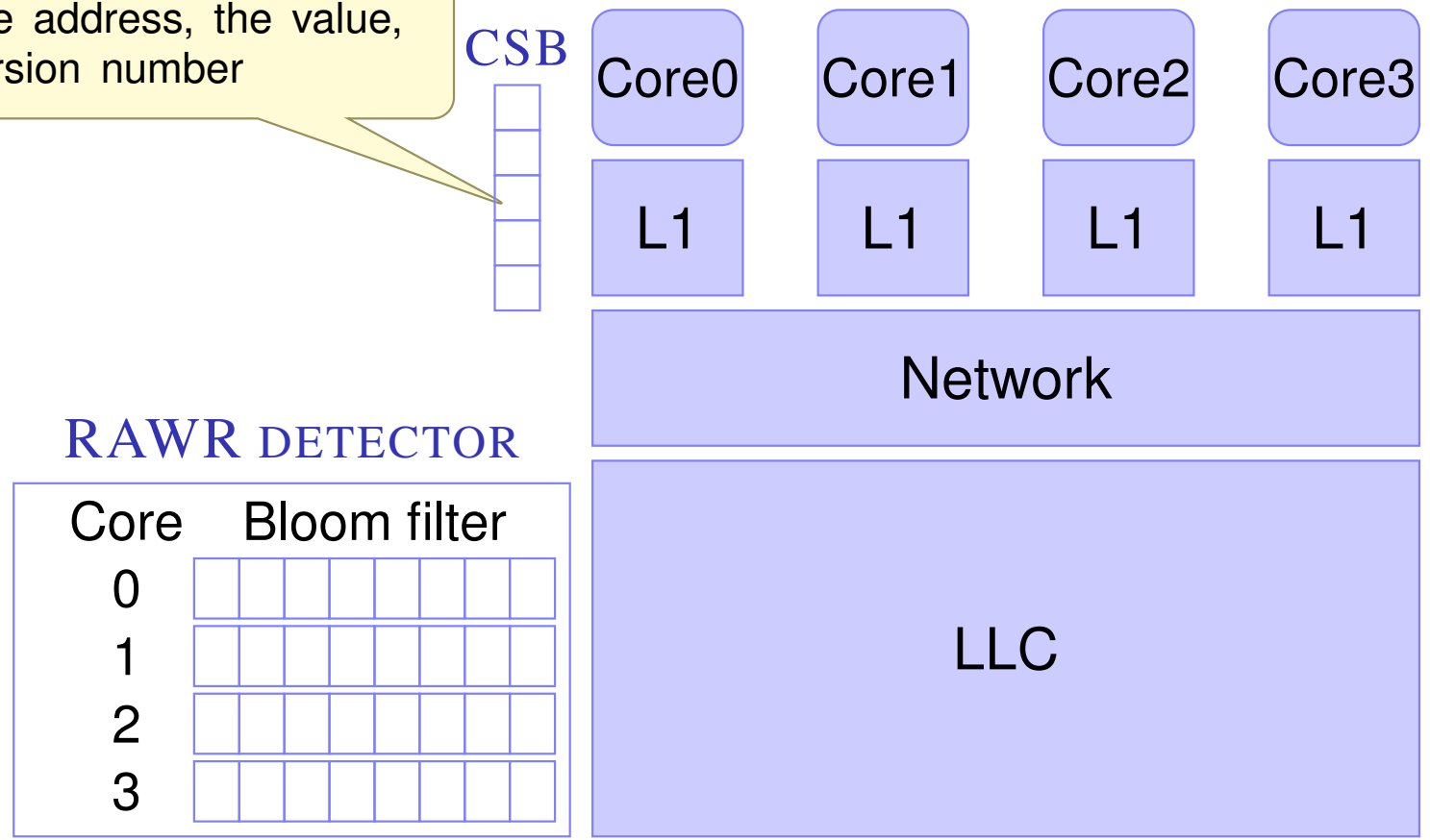
Optimizing write-back traffic



Optimizing write-back traffic

Local coalescing store buffer (CSB)

- Stores the address, the value, and a version number



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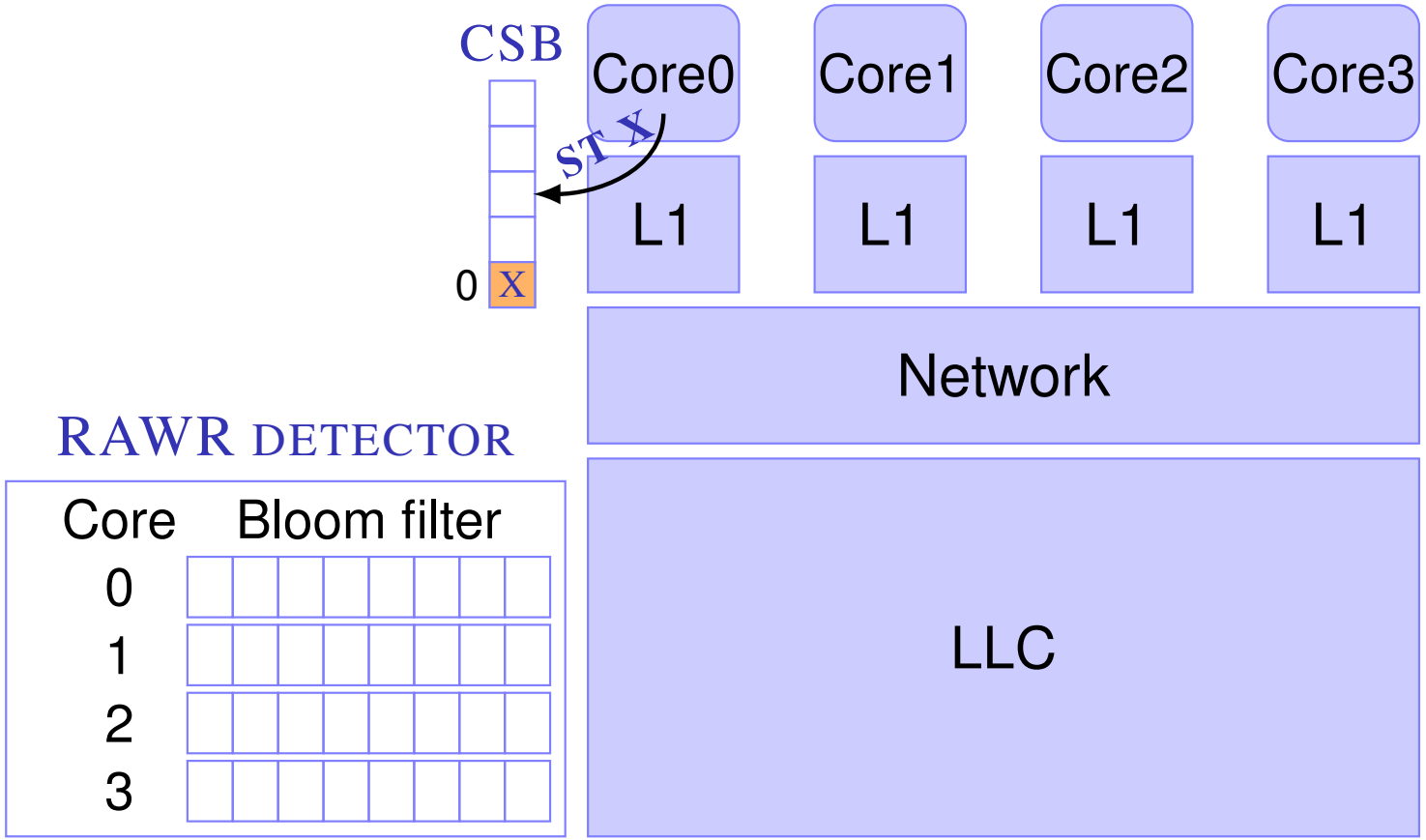
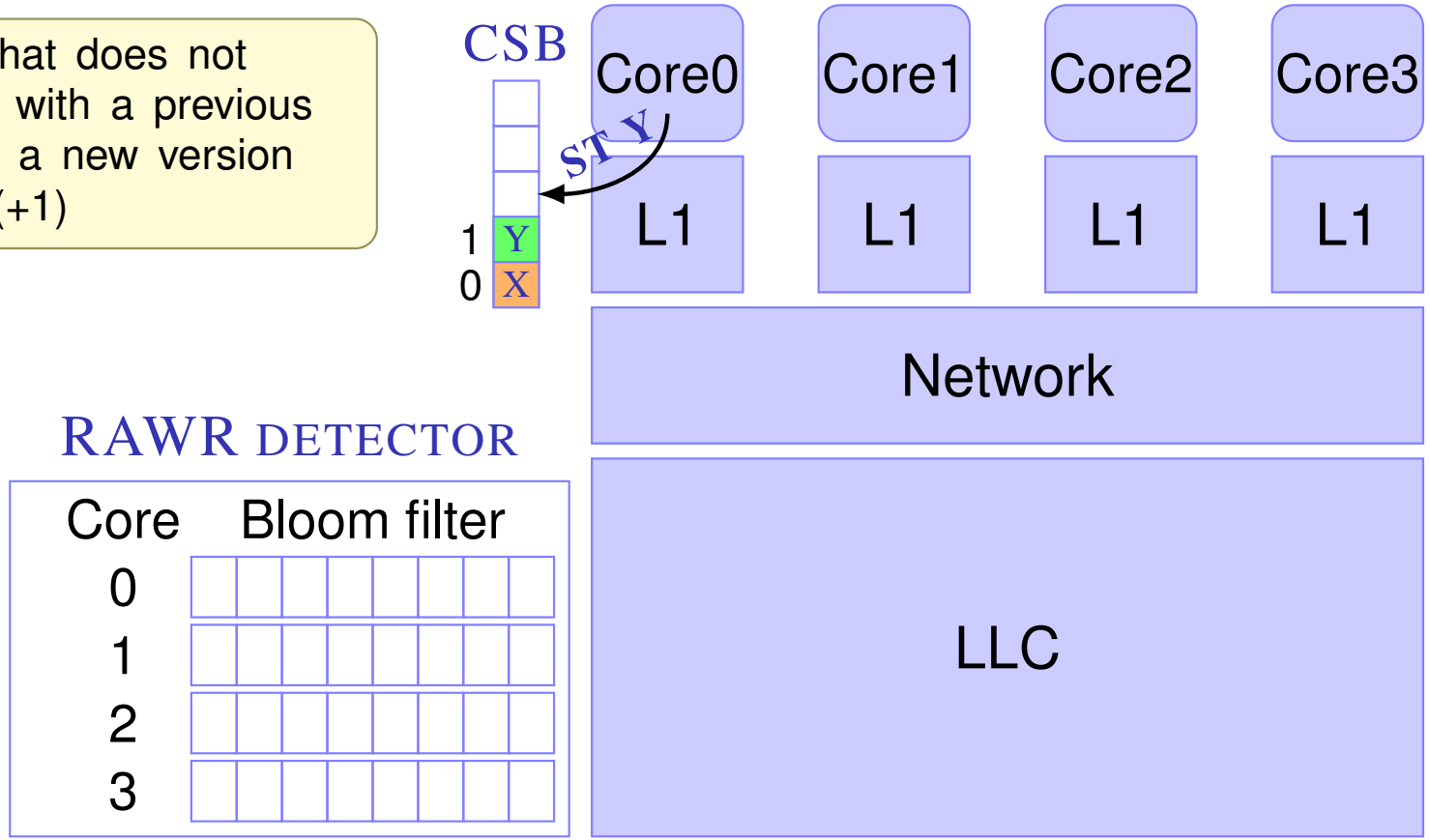


Optimizing write-back traffic

A write that does not coalesce with a previous one gets a new version number (+1)



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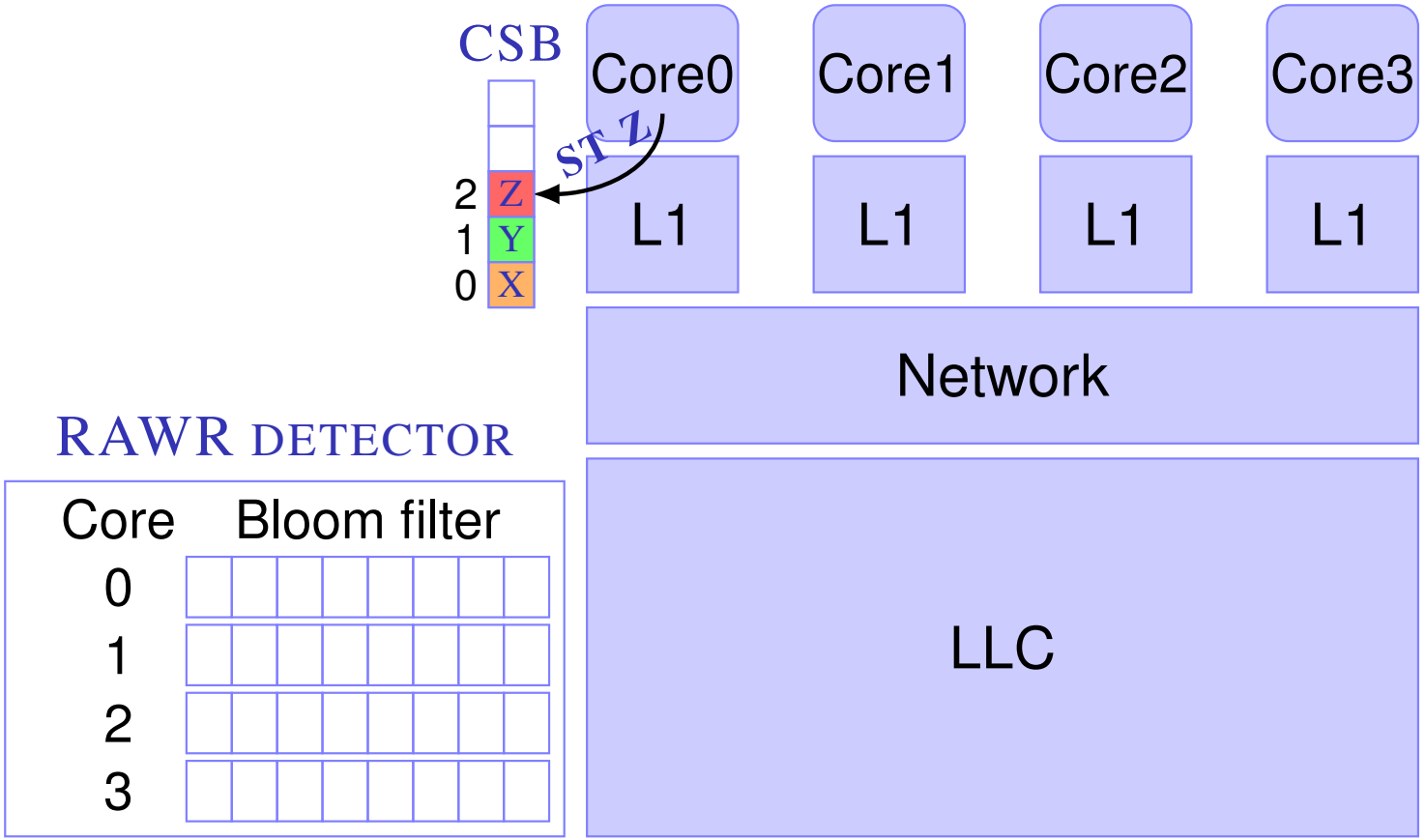
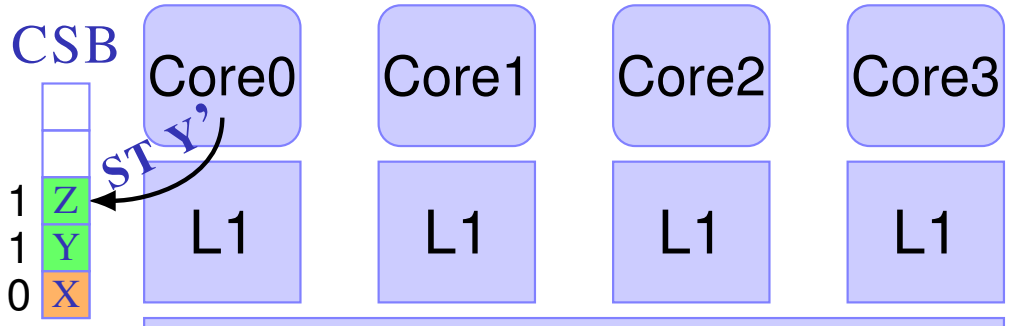


Optimizing write-back traffic

A write that coalesces forces all version numbers between the last one and the coalesced one to be same (e.g., coalesced order 1)



RAWR detector

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0	
1	
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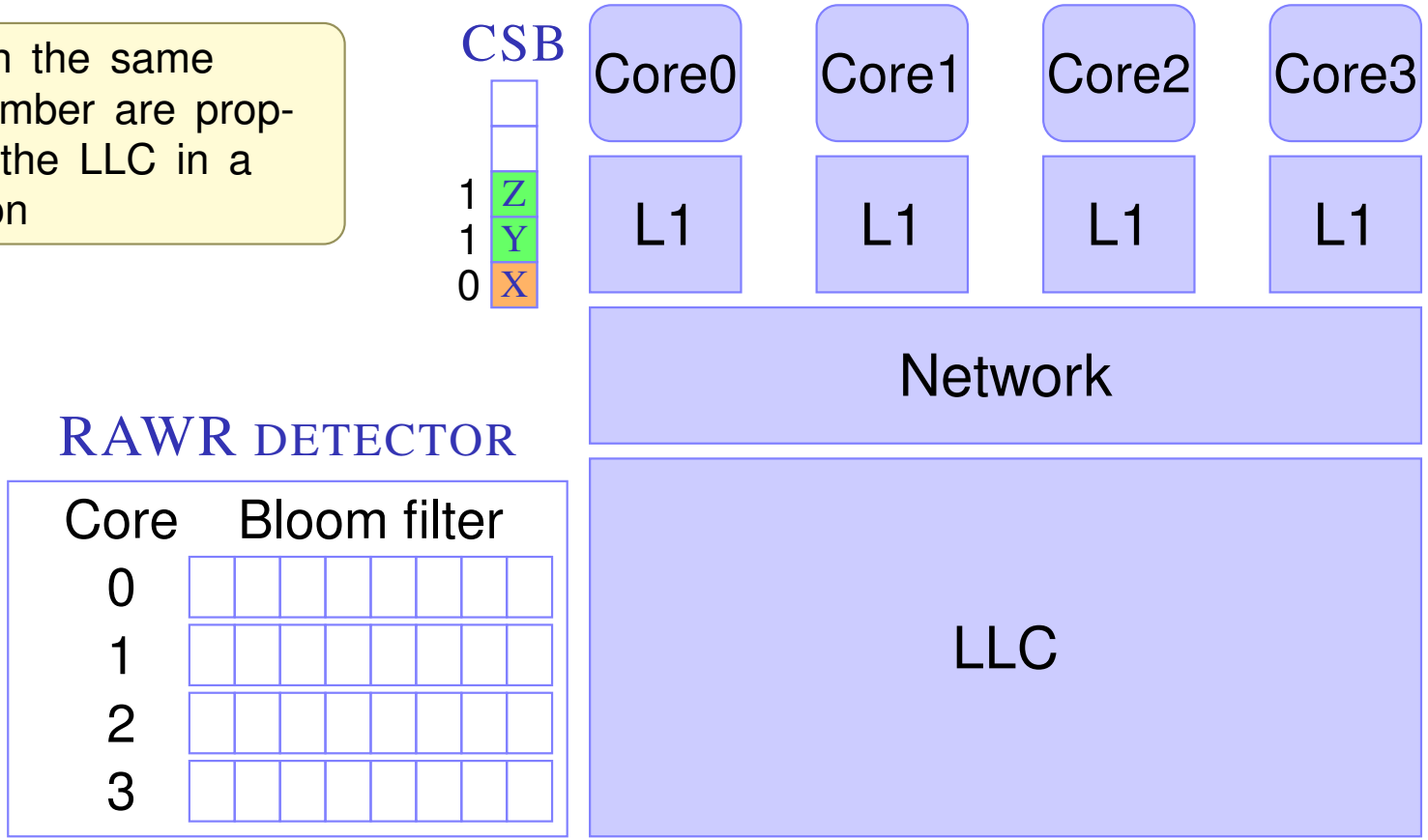
Writes with the same version number are propagated to the LLC in a bulk fashion



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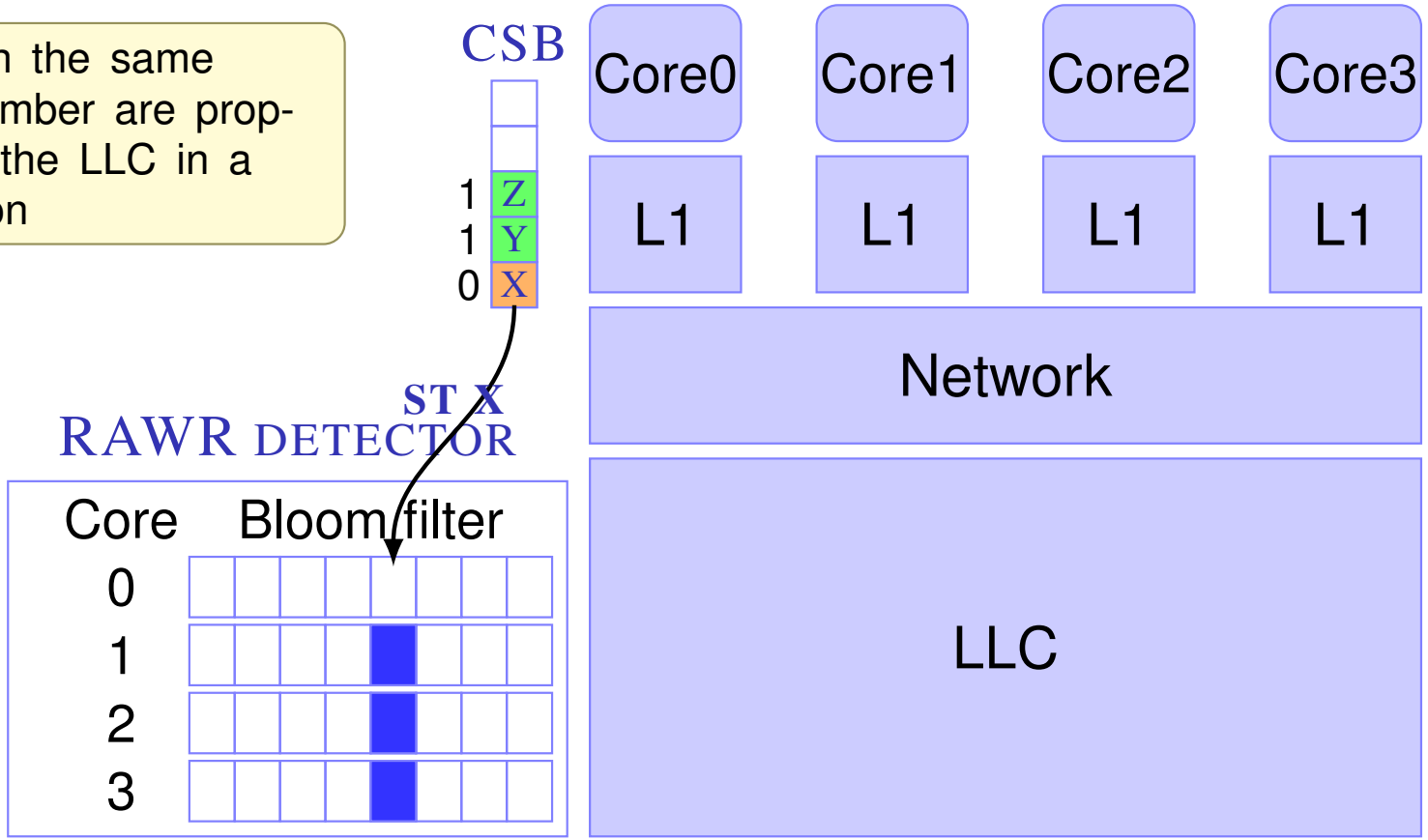

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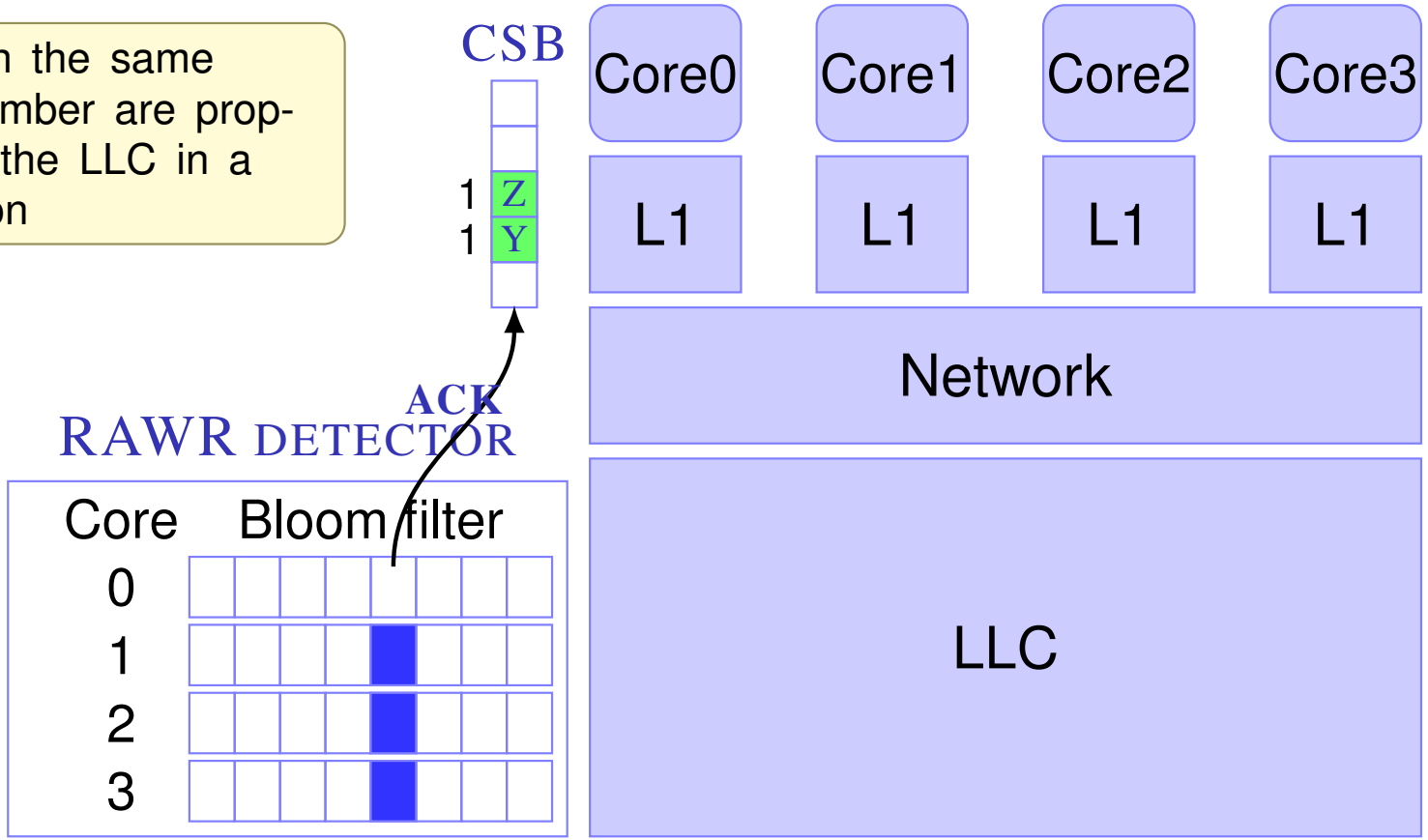
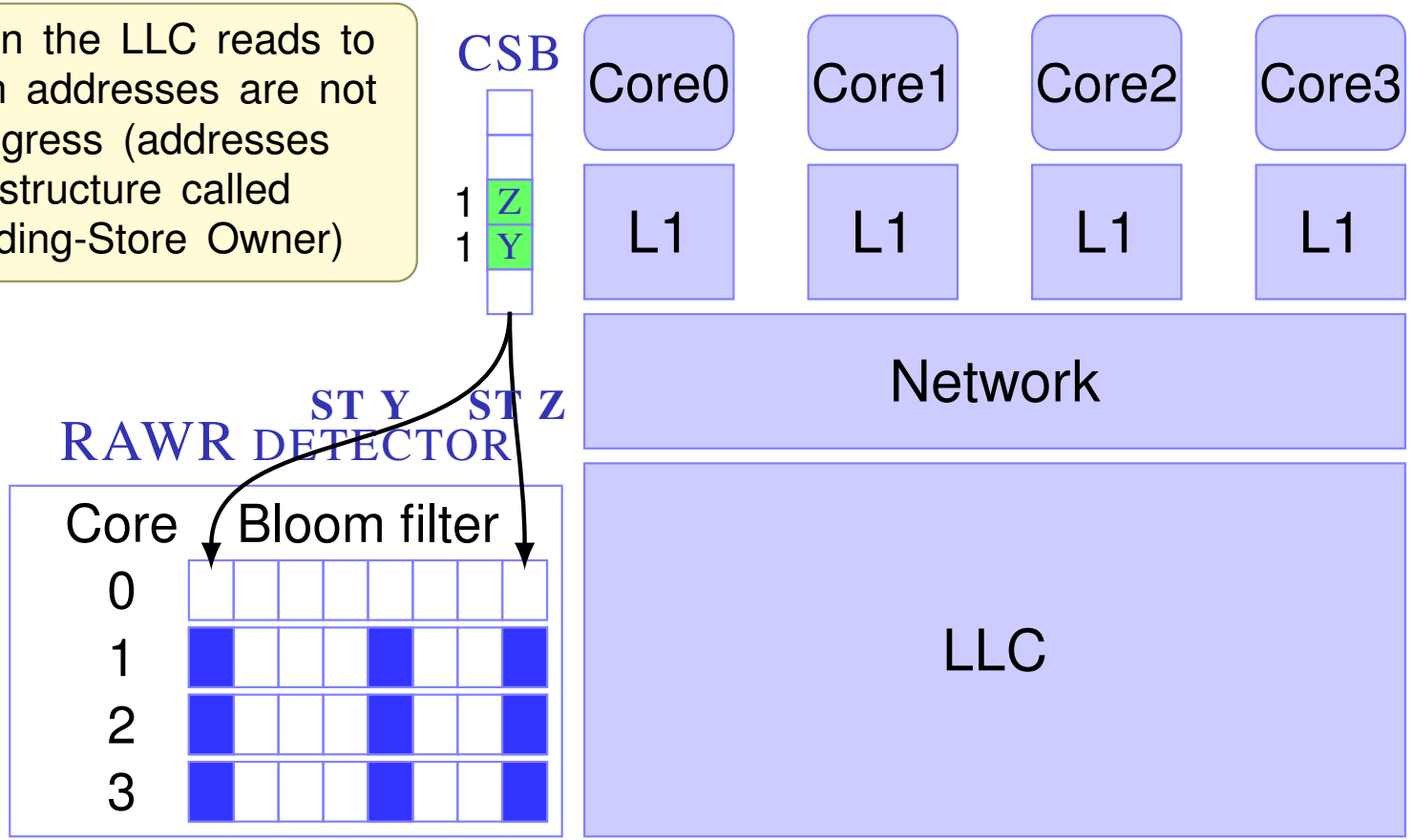


Optimizing write-back traffic

While writing in the LLC reads to already written addresses are not allowed to progress (addresses tracked in an structure called OSO, Outstanding-Store Owner)



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