Curriculum Vitae

February'2025

Juan L. Aragón
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CONTACT

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SUMMARY

Juan L. Aragón is a Full Professor in Computer Architecture at the University of Murcia (Spain). He received his M.Sc. degree in Computer Science in 1996 and his Ph.D. degree in Computer Engineering in 2003, both from the University of Murcia (Spain). In 1999 he joined the Computer Engineering Department at the University of Murcia as an Assistant Professor. In 2003-2004, he did a 1-year post-doctoral stay as a Visiting Assistant Professor and Researcher in the Computer Science Department at the University of California, Irvine. He has also been a Visiting Researcher at EPFL (Lausanne, Switzerland) in 2013; and a Visiting Researcher at Princeton University (NJ, USA) in 2015, 2017, 2018, 2019 and 2022. His research interests are focused on computer architecture, energy-efficient processors, microarchitecture design, accelerators, heterogeneous systems, GPUs, in addition to more applied research in the field of human visual optics. Dr. Aragón has advised 7 Ph.D. theses and has co-authored +80 research papers in major conferences and journals in computer architecture.

EDUCATION

Oct'99 – Feb'03 — *Ph.D. in Computer Engineering*
Computer Engineering Department, Universidad de Murcia (Spain)
Advisors: José González (UMU) and Antonio González (UPC)

Oct'94 – June'96 — *M.S. in Computer Science*
Facultad de Informática, Universidad de Murcia

Oct'91 – June'94 — *B.S. in Computer Science*
Facultad de Informática, Universidad de Murcia

EXPERIENCE

July'22 – *present* — *Full Professor*
Computer Engineering Department, Universidad de Murcia (Spain)

Master-level Teaching:
- "Advanced Aspects on General Purpose Multicore Architectures" (2022-2024)

Undergraduate-level Teaching:

- "Computer Architecture" (2nd year) (2022-2024)
- "Advanced Computer Architecture" (3rd year) (2022-2024)

Oct'07 – July'22 *Associate Professor*
Computer Engineering Department, Universidad de Murcia (Spain)

Master-level Teaching:

- "Advanced Aspects on General Purpose Multicore Architectures" (2010-2022)
- "Technologies and Architectures for Embedded Systems" (2007-2010)

Undergraduate-level Teaching:

- "Computer Architecture" (2nd year) (2007-2022)
- "Advanced Computer Architecture" (3rd year) (2011-2022)
- "Introduction to Computer Organization" (2007-2009)
- "Operating Systems" (2009)

Jul'24 – Ago'24 *Visiting Researcher*
Department of Electrical, Electronic, and Information Engineering, Università di Bologna (Italy), PULP Lab research group, headed by Prof. Luca Benini

Jul'23 – Ago'23 *Visiting Researcher*
Computer Architecture Department, Universitat Politécnica de Catalunya (Spain)
ARCO research group, headed by Prof. Antonio González

Feb'22 – June'22 *Visiting Researcher*
Dept. of Computer Science, Princeton University (NJ, USA)
MRM research group, headed by Prof. Margaret Martonosi

Feb'19 – June'19 *Visiting Researcher*
Dept. of Computer Science, Princeton University (NJ, USA)
MRM research group, headed by Prof. Margaret Martonosi

Mar'18 – July'18 *Visiting Researcher*
Dept. of Computer Science, Princeton University (NJ, USA)
MRM research group, headed by Prof. Margaret Martonosi

Oct'15 – Dec'17 *Department Chair*
Computer Engineering Department, Universidad de Murcia (Spain)

Jul'17 – Aug'17 *Visiting Researcher*
Dept. of Computer Science, Princeton University (NJ, USA)
MRM research group, headed by Prof. Margaret Martonosi

Feb'15 – July'15 *Visiting Researcher*
Dept. of Computer Science, Princeton University (NJ, USA)
MRM research group, headed by Prof. Margaret Martonosi

Mar'13 – July'13 *Visiting Researcher*
IC School, EPFL University (Switzerland)
PARSA research group, headed by Prof. Babak Falsafi

May'06 – Sep'08 *Vice Dean for Student Affairs*
Facultad de Informática, Universidad de Murcia (Spain)

Oct'99 – Oct'07 *Assistant Professor*
Computer Engineering Department, Universidad de Murcia (Spain)

Undergraduate Courses:
- Introduction to Computer Organization (1999-2007)
- Logic Design and Digital Systems (1999-2003)
- Computer Architecture (2004-2007)

Master Courses:
- Grid Computing (year 2004)
- High Performance Architectures for Embedded Systems (2005)
- Technologies and Architectures for Embedded Systems (2006-2007)

June'03 – June'04 *Visiting Assistant Professor and Researcher*
Computer Science Dept., University of California, Irvine (CA, USA)

Undergraduate Courses:
- ICS-152: Computer Systems Architecture (Fall-2003 and Winter-2004)

Sep'97 – Sep'99 *Graduate Researcher*
Physics Department, Universidad de Murcia (Spain)
I was involved in several research projects in the Optics Research Group, developing several real-time systems to analyze and process digital images from the human retina.

Mar 1, 99 – Apr 30, 99 Internship at the Center for Visual Science, University of Rochester (NY, USA)
Developing a real-time digital image processing application to determine the ocular wave aberration of the human eye.

May'97 – Sep'97 *Systems Manager*
Computer Science Department, Universidad de Murcia (Spain)
Managing a cluster of Sun UltraSparc-I workstations and working in parallel algorithms using High Performance Fortran (HPF).

FELLOWSHIPS & GRANTS RECEIVED

Feb'22 – June'22 Research Mobility Fellowship (Beca para Estancias Externas de Investigadores. Programa de Movilidad Jiménez de la Espada-2021)
Granted by Fundación Séneca, Región de Murcia (Spain) (12450€)

Mar'19 – May'19 Research Mobility Fellowship (Beca para Estancias Externas de Investigadores. Programa de Movilidad Jiménez de la Espada-2018)
Granted by Fundación Séneca, Región de Murcia (Spain) (7950€)

Feb'15 – July'15 Research Mobility Fellowship (Estancias de movilidad de profesores e investigadores senior en centros extranjeros de enseñanza superior e investigación, incluido el Programa Salvador de Madariaga-2014)
Granted by Ministerio de Educación, Cultura y Deporte (Spain) (19300€)

Mar'13 – July'13	Research Mobility Fellowship (Beca para Estancias Externas de Investigadores. Programa de Movilidad Jiménez de la Espada-2012) Granted by Fundación Séneca, Región de Murcia (Spain) (6600€)
Sep'10 – Dec'10	HiPEAC Collaboration Grant: "Effects of a temperature-aware scheduler in a 3D-stacked architecture", in collaboration with Prof. Stefanos Kaxiras (University of Uppsala). Granted by HiPEAC-2 European Network of Excellence (5000€)
Sep'10 – Dec'10	HiPEAC Collaboration Grant: "The Implications of Near Threshold Last Level Cache Operation for Parallel Workloads", in collaboration with Prof. Yiannakis Sazeides (Univ. Cyprus). Granted by HiPEAC-2 EU Network of Excellence (5000€)
Dec'07 – May'08	HiPEAC Research Cluster #1173: "Efficient microarchitectural policies under power constraints at minimal performance cost", in collaboration with Prof. Stefanos Kaxiras. Granted by HiPEAC European Network of Excellence (7500€)
May'05 – July'05	HiPEAC Research Cluster #355: "Energy-efficient single-core processor design", in collaboration with Prof. Stefanos Kaxiras (University of Patras, Greece) Granted by HiPEAC European Network of Excellence (4000€)
June'03 – June'04	1-year Post-doctoral Fellowship (Beca de Formación Post-doctoral) Granted by Fundación Séneca, Región de Murcia (Spain)
Sep'97 – Sep'99	2-year Pre-doctoral Fellowship (Beca FPI de Formación Pre-doctoral) Granted by Fundación Séneca, Región de Murcia (Spain)

PUBLICATIONS

JOURNALS:

[J.1] A. Vicente-Jaén, J. Mompeán, J.L. Aragón and P. Artal. "VolRec: 4D real-time volumetric reconstruction of OCT data". *The Journal of Supercomputing*, vol. 81, no. 472, pp. 1-22, ISSN: 0920-8542, February 2025

[J.2] A. Manocha, J.L. Aragón and M. Martonosi. "Graphfire: Synergizing Fetch, Insertion, and Replacement Policies for Graph Analytics". *IEEE Transactions on Computers*, vol. 72, issue 1, pp. 291-304, ISSN: 0018-9340, January 2023

[J.3] D. Corbalán-Navarro, J.L. Aragón, M. Anglada, E. de Lucas, J.M. Parcerisa and A. González. "Omega-Test: A Predictive Early-Z Culling to Improve the Graphics Pipeline Energy-Efficiency". *IEEE Transactions on Visualization and Computer Graphics*, vol. 28, issue 14, pp. 4375-4388, ISSN: 1077-2626, December 2022

[J.4] D. Corbalán-Navarro, J.L. Aragón, M. Anglada, J.M. Parcerisa and A. González. "Triangle Dropping: An Occluded-Geometry Predictor for Energy-efficient Mobile GPUs". *ACM Transactions on Architecture and Code Optimization*, vol. 19, issue 3, article 39, pp. 1-20, ISSN: 1544-3566, September 2022

[J.5] M. Anglada, E. de Lucas, J.M. Parcerisa, J.L. Aragón and A. González. "Dynamic Sampling Rate: Harnessing Frame Coherence in Graphics Applications for Energy-Efficient GPUs". *The Journal of Supercomputing*, vol. 78, issue 13, pp. 14940-14964, ISSN: 0920-8542, September 2022

[J.6] J. Mompeán, J.L. Aragón and P. Artal. "Energy-efficient design of a presbyopia correction wearable powered by mobile GPUs and FPGAs". *The Journal of Supercomputing*, vol. 78, no. 9, pp. 11657–11679, ISSN: 0920-8542, June 2022

[J.7] A. Manocha, T. Sorensen, E. Tureci, O. Matthews, J.L. Aragón and M. Martonosi. "GraphAttack: A Hardware-Software Data Supply Optimization for Graph Applications on In-Order Multicore Architectures". *ACM Transactions on Architecture and Code Optimization*, vol. 18, issue 4, article 53, pp 1-26, ISSN: 1544-3566, December 2021

[J.8] M. Anglada, R. Canal, J.L. Aragón and A. González. "Fast and Accurate SER Estimation for Large Combinational Blocks in Early Stages of the Design". *IEEE Transactions on Sustainable Computing*, vol. 6, issue 3, pp. 427–440, ISSN: 2377-3782, July-Sept 2021

[J.9] J. Mompeán, J.L. Aragón and P. Artal. "Portable device for presbyopia correction with optoelectronic lenses driven by pupil response". *Scientific Reports*, vol. 10, no. 20293, pp. 1-9, ISSN: 2045-2322, November 2020

[J.10] T.J. Ham, J.L. Aragón and M. Martonosi. "Efficient Data Supply for Parallel Heterogeneous Architectures". *ACM Transactions on Architecture and Code Optimization*, vol. 16, issue 2, article 9, pp. 1-23, ISSN: 1544-3566, April 2019

[J.11] J. Mompeán, J.L. Aragón, P. Prieto and P. Artal. "GPU-based processing of Hartmann-Shack images for accurate and high-speed ocular wavefront sensing". *Future Generation Computer Systems*, vol. 91, pp. 177–190, ISSN: 0167-739X, February 2019

[J.12] J. Mompeán, J.L. Aragón, P. Prieto and P. Artal. "Design of an Accurate and High-Speed Binocular Pupil Tracking System based on GP-GPUs". *The Journal of Supercomputing*, vol. 74, no. 5, pp. 1836–1862, ISSN: 0920-8542, May 2018

[J.13] T.J. Ham, J.L. Aragón and M. Martonosi. "Decoupling Data Supply from Computation for Latency-Tolerant Communication in Heterogeneous Architectures". *ACM Transactions on Architecture and Code Optimization*, vol. 14, issue 2, article 16, ISSN: 1544-3566, July 2017

[J.14] J. Mompeán, J.L. Aragón, S. Manzanera and P. Artal, "Presbyopia Correction with Optoelectronic Lenses Driven by Pupil Size". *Investigative Ophthalmology & Visual Science*, vol. 57, no. 12, ISSN: 1552-5783, September 2016

[J.15] T.J. Ham, J.L. Aragón and M. Martonosi. "DeSC: Decoupled Supply-Compute Communication Management for Heterogeneous Architectures". *IEEE MICRO*, *Special issue: Top Picks from the 2015 Computer Architecture Conferences,* ***with Honorable Mention***, vol. 36, no. 3, pp. 7, ISSN: 0272-1732, May-June 2016

[J.16] D. Sánchez, J.M. Cebrián, J.M. García and J.L. Aragón. "Soft-Error Mitigation by means of Decoupled Transactional Memory Threads". *Distributed Computing*, vol. 28, no. 2, pp. 75-90, ISSN: 0178-277, April 2015

[J.17] J.M. Cebrián, D. Sánchez, J.L. Aragón and S. Kaxiras. "Managing Power Constraints in a Single-core Scenario through Power Tokens". *The Journal of Supercomputing*, vol. 68, no. 1, pp. 414-442, ISSN: 0920-8542, April 2014

[J.18] D. Sánchez, Y. Sazeides, J.M. Cebrián, J.M. García and J.L. Aragón. "Modelling the impact of permanent faults in caches". *ACM Transactions on Architecture and Code Optimization*, vol. 10, issue 4, article 29, pp. 1-23, ISSN: 1544-3566, December 2013

[J.19] J.M. Cebrián, D. Sánchez, J.L. Aragón and S. Kaxiras. "Efficient Inter-core Power and Thermal Balancing for Multicore Processors". *Computing*, vol. 95, no. 7, pp. 537-566, ISSN: 0010-485X, July 2013

[J.20] D. Sánchez, J.L. Aragón and J.M. García. "A Fault-Tolerant Architecture for Parallel Applications in Tiled-CMPs". *The Journal of Supercomputing*, vol. 61, no. 3, pp. 997-1023, ISSN: 0920-8542, September 2012

[J.21] J.M. Cebrián, J.L. Aragón, J.M. García and S. Kaxiras. "Leakage-efficient Design of Value Predictors through State and Non-state Preserving Techniques". *The Journal of Supercomputing*, vol. 55, no. 1, pp. 28-50, ISSN: 0920-8542, January 2011

[J.22] A. Flores, M.E. Acacio and J.L. Aragón. "Exploiting Address Compression and Heterogeneous Interconnects for Efficient Message Management in Tiled CMPs". *Journal of Systems Architecture*, vol. 56, no. 9, pp. 429-441, ISSN: 1383-7621, September 2010

[J.23] A. Flores, J.L. Aragón and M.E. Acacio. "Heterogeneous Interconnects for Energy-Efficient Message Management in CMPs". *IEEE Transactions on Computers*, vol. 59, no. 1, pp. 16-28, ISSN: 0018-9340, January 2010

[J.24] J.L. Aragón and A. Veidenbaum. "Optimizing CAM-Based Instruction Cache Designs for Low-Power Embedded Systems". *Journal of Systems Architecture*, vol. 54, no. 12, pp. 1155-1163, ISSN: 1383-7621, December 2008

[J.25] A. Flores, J.L. Aragón and M.E. Acacio. "An Energy Consumption Characterization of On-Chip Interconnection Networks for Tiled CMP Architectures". *The Journal of Supercomputing*, vol. 45, no. 3, pp. 341-364, ISSN: 0920-8542, September 2008

[J.26] J.L. Aragón, J. González and A. González. "Control Speculation for Energy-Efficient Next-Generation Superscalar Processors". *IEEE Transactions on Computers,* vol. 55, no. 3, pp. 281-291, ISSN: 0018-9340, March 2006

[J.27] J.L. Aragón, J. González and A. González. "Reducing Branch Misprediction Penalty through Confidence Estimation". *Journal of Computer Science & Technology,* vol. 3, no. 1, ISSN: 1666-6038, April 2003

CONFERENCES:

[C.1] A. Tomás, J.L. Aragón, J.M. Parcerisa and A. González. "LIBRA: Memory Bandwidth- and Locality-Aware Parallel Tile Rendering". *Proc. of the 57th ACM/IEEE International Symposium on Microarchitecture* (**MICRO**), Austin, Texas, USA, pp. 1058-1072, ISBN: 979-8-3503-5057-9, November 2024

[C.2] A. Manocha, Z. Yan, E. Tureci, J.L. Aragón, David Nellans and M. Martonosi. "Architectural Support for Optimizing Huge Page Selection Within the OS". *Proc. of the 56th ACM/IEEE International Symposium on Microarchitecture* (**MICRO**), Toronto, Canada, pp. 1-14, ISBN: 979-8-4007-0329-4, October 2023

[C.3] D. Joseph, J.L. Aragón, J.M. Parcerisa and A. González. "Boustrophedonic Frames: Quasi-Optimal L2 Caching for Textures in GPUs". *Proc. of the 32nd International Conference on Parallel Architectures and Compilation Techniques* (**PACT**), pp. 1-13, Viena, Austria, October 2023

[C.4] A. Manocha, Z. Yan, E. Tureci, J.L. Aragón, David Nellans and M. Martonosi. "The Implications of Page Size Management on Graph Analytics". *Proc. of the 2022 IEEE International Symposium on Workload Characterization* (**IISWC**), Austin, Texas, USA, pp. 199-214, ISBN: 978-1-6654-8798-6, November 2022

[C.5] D. Joseph, J.L. Aragón, J.M. Parcerisa and A. González. "DTexL: Decoupled Raster Pipeline for Texture Locality". *Proc. of the 55th ACM/IEEE International Symposium on Microarchitecture* (**MICRO**), Chicago, Illinois, USA, pp. 213-227, ISBN: 978-1-6654-6272-3, October 2022

[C.6] A.M. Paniagua-Diaz, J. Mompeán, J.L. Aragón and P. Artal. "Adaptive optics visual simulation using economic and compact vertical aligned liquid crystal devices". *Proc. of the Imaging and Applied Optics Congress 2022, Adaptive Optics and Applications*, Vancouver, British Columbia, Canada, ISBN: 978-1-957171-09-8, July 2022

[C.7] M. Orenes-Vera, A. Manocha, J. Balkind, F. Gao, J.L. Aragón, D. Wentzlaff and M. Martonosi. "Tiny but Mighty: Designing and Realizing Scalable Latency Tolerance for Manycore SoCs". *Proc. of the 49th IEEE/ACM International Symposium on Computer Architecture* (**ISCA**), New York, NY, USA, pp. 817-830, ISBN: 978-1-4503-8610-4, June 2022. ***Also selected for IEEE MICRO Top Picks from the 2022 Computer Architecture Conferences, with Honorable Mention***

[C.8] J. Ortiz-Escribano, D. Corbalán-Navarro, J.L. Aragón and A. González. "MEGsim: A Novel Methodology for Efficient Simulation of Graphics Workloads in GPUs". *Proc. of the 2022 IEEE International Symposium on Performance Analysis of Systems and Software* (**ISPASS**), Singapore, Singapore, pp. 69-78, ISBN: 978-1-6654-5954-9, May 2022

[C.9] D. Joseph, J.L. Aragón, J.M. Parcerisa and A. González. "TCOR: A Tile Cache with Optimal Replacement". *Proc. of the 28th IEEE Int. Symposium on High-Performance Computer Architecture* (**HPCA**), Seoul, South Korea, pp. 662-675, ISBN: 978-1-6654-2027-3, April 2022

[C.10] D. Corbalán-Navarro, J.L. Aragón, J.M. Parcerisa and A. González. "DTM-NUCA: Dynamic Texture Mapping-NUCA for Energy-Efficient Graphics Rendering". *Proc. of the 30th IEEE Euromicro International Conference on Parallel, Distributed and Network-based Computing* (**PDP**), Valladolid, Spain, pp. 144-151, ISBN: 978-1-6654-6958-6, March 2022

[C.11] T. Sorensen, A. Manocha, E. Tureci, M. Orenes-Vera, J.L. Aragón and M. Martonosi. "A Simulator and Compiler Framework for Agile Hardware-Software Co-design Evaluation and Exploration". *Proc. of the 2020 IEEE/ACM Int. Conference on Computer Aided Design* (**ICCAD**), San Diego, CA, USA, pp. 1-9, ISBN: 978-1-4503-8026-3, November 2020

[C.12] O. Matthews, A. Manocha, D. Giri, M. Orenes-Vera, E. Tureci, T. Sorensen, T.J. Ham, J.L. Aragón, L.P. Carloni and M. Martonosi. "MosaicSim: A Lightweight, Modular Simulator for Heterogeneous Systems". *Proc. of the 2020 IEEE Int. Symposium on Performance Analysis of Systems and Software* (**ISPASS**), Boston, MA, USA, pp. 136-148, ISBN: 978-1-7281-4798-7, August 2020, ***Nominated for Best Paper***

[C.13] T.J. Ham, J.L. Aragón and M. Martonosi. "Efficient Data Supply for Parallel Heterogeneous Architectures". *Presented at the 15th Int. High Performance and Embedded Architecture and Compilation Conference* (**HiPEAC**), Bologna, Italy, January 2020

[C.14] M. Anglada, E. de Lucas, J.M. Parcerisa, J.L. Aragón and A. González. "Early Visibility Resolution for Removing Ineffectual Computations in the Graphics Pipeline". *Proc. of the 25th IEEE Int. Symposium on High-Performance Computer Architecture* (**HPCA**), Washington D.C., USA, pp. 635-646, ISBN: 978-1-7281-1444-6, February 2019

[C.15] M. Anglada, E. de Lucas, J.M. Parcerissa, J.L. Aragón, P. Marcuello and A. González. "Rendering Elimination: Early Discard of Redundant Tiles in the Graphics Pipeline". *Proc. of the 25th IEEE Int. Symposium on High-Performance Computer Architecture* (**HPCA**), Washington D.C., USA, pp. 623-634, ISBN: 978-1-7281-1444-6, February 2019

[C.16] M. Anglada, R. Canal, J.L. Aragón and A. González. "MASkIt: Soft Error Rate Estimation for Combinational Circuits". *Proc. of the 34th IEEE Int. Conference on Computer Design* (**ICCD**), Phoenix, USA, pp. 614-621, ISBN: 978-1-5090-5135-9, October 2016

[C.17] T.J. Ham, J.L. Aragón and M. Martonosi. "DeSC: Decoupled Supply-Compute Communication Management for Heterogeneous Architectures". *Proc. of the 48th IEEE/ACM Int. Symposium on Microarchitecture* (**MICRO**), Hawaii, USA, pp. 191-203, ISBN: 978-1-4503-4034-2, Dec. 2015 ***Also selected for IEEE MICRO Top Picks from the 2015 Computer Architecture Conferences, with Honorable Mention***

[C.18] J. Mompeán, J.L. Aragón, P. Prieto and P. Artal. "GPU-accelerated High-speed Eye Pupil Tracking System". *Proc. of the 27th IEEE Int. Symposium on Computer Architecture and High-Performance Computing* (**SBAC-PAD**), Florianópolis, Brazil, pp. 20-27, ISBN: 978-1-4673-8011-9, Oct 2015

[C.19] J.M. Cebrián, J.L. Aragón and S. Kaxiras. "Token3D: Reducing Temperature in 3D die-stacked CMPs through Cycle-level Power Control Mechanisms". *Proc. of the 17th Int. Conference on Parallel and Distributed Computing* (**Euro-Par**), Bordeaux, France, pp. 295-309, ISBN: 978-3-642-23399-9. *Lecture Notes in Computer Science*, vol. 6852, Springer-Verlag, pp. 295-309, ISSN: 0302-9743, August 2011

[C.20] D. Sánchez, Y. Sazeides, J.L. Aragón and J.M. García. "An Analytical Model for the Calculation of the Expected Miss Ratio in Faulty Caches". *Proc. of the 17th IEEE International On-Line Testing Symposium* (**IOLTS**), Athens, Greece, pp. 287-292, ISBN: 978-1-4577-1054-4, July 2011

[C.21] J.M. Cebrián, J.L. Aragón and S. Kaxiras. "Power Token Balancing: Adapting CMPs to Power Constraints for Parallel Multithreaded Workloads". *Proc. of the 25th IEEE Int. Parallel and Distributed Processing Symposium* (**IPDPS**), Anchorage, Alaska, USA, pp. 431-442, ISBN: 978-0-7695-4385-7, May 2011

[C.22] D. Sánchez, J.L. Aragón and J.M. García. "A Log-Based Redundant Architecture for Reliable Parallel Computation". *Proc. of the 17th IEEE Int. Conference on High Performance Computing* (**HiPC**), Goa, India, pp. 79-88, ISBN: 978-1-4244-8519-2, December 2010

[C.23] P. Petoumenos, G. Psychou, S. Kaxiras, J.M. Cebrián and J.L. Aragón. "MLP-aware Instruction Queue Resizing: The Key to Power-Efficient Performance". *Proc. of the 23rd Int. Conference on Architecture of Computing Systems* (**ARCS**), Hannover, Germany. *Lecture Notes in Computer Science*, vol. 5974, Springer-Verlag, pp. 113-125, ISSN: 0302-9743, February 2010

[C.24] A. Flores, J.L. Aragón and M.E. Acacio. "Energy-Efficient Hardware Prefetching for CMPs using Heterogeneous Interconnects". *Proc. of the 18th IEEE Euromicro International Conference on Parallel, Distributed and Network-Based Computing* (**EUROMICRO-PDP**), Pisa, Italy, pp. 147-154, ISBN: 978-1-4244-5672-7, February 2010

[C.25] K.E. Østby, J.L. Aragón, J.M. García and M. Ujaldón. "FATSEA – An Architectural Simulator for General Purpose Computing on GPUs". *Proc. of the 2nd Workshop on Rapid Simulation & Performance Evaluation: Methods and Tools* (**RAPIDO**), *in conjunction with HiPEAC'10*, Pisa, Italy, pp. 1-6, ISBN: 3-642-11514-4, January 2010

[C.26] D. Sánchez, J.L. Aragón and J.M. García. "REPAS: Reliable Execution for Parallel Applications in Tiled-CMPs". *Proc. of the 15th Int. Conference on Parallel and Distributed Computing* (**Euro-Par**), Delft, Netherlands, pp. 321-333, ISBN: 978-3-642-03868-6. *Lecture Notes in Computer Science*, vol. 5704, Springer-Verlag, pp. 321-333, ISSN: 0302-9743, August 2009

[C.27] J.M. Cebrián, J.L. Aragón, J.M. García, P. Petoumenos and S. Kaxiras. "Efficient Microarchitecture Policies for Accurately Adapting to Power Constraints". *Proc. of the 23rd IEEE Int. Parallel and Distributed Processing Symp.* (**IPDPS**), Rome, Italy, pp. 1-12, ISBN: 978-1-4244-3750-4, May 2009

[C.28] D. Sánchez, J.L. Aragón and J.M. García. "Extending SRT for Parallel Applications in Tiled-CMP Architectures". *Proc. of the 14th IEEE Workshop on Dependable Parallel, Distributed and Network-Centric Systems* (**DPDNS**), *in conjunction with IPDPS'09*, Rome, Italy, pp. 1-10, ISBN: 978-1-4244-3750-4, May 2009

[C.29] A. Flores, M.E. Acacio and J.L. Aragón. "Address Compression and Heterogeneous Interconnects for Energy-Efficient High-Performance in Tiled CMPs". *Proc. of the 37th IEEE Int. Conference on Parallel Processing* (**ICPP**), Portland, OR, USA, pp. 295-303, ISBN: 978-0-7695-3374-2, Sep. 2008

[C.30] D. Sánchez, J.L. Aragón and J.M. García. "Evaluating Dynamic Core Coupling in a Scalable Tiled-CMP Architecture". *Proc. of the 7th Int. Workshop on Duplicating, Deconstructing, and Debunking* (**WDDD**), *in conj. with ISCA'08*, Beijing, China, pp. 1-10, ISBN: 978-0-7695-3174-8, June 2008

[C.31] A. Flores, J.L. Aragón and M.E. Acacio. "Efficient Message Management in Tiled CMP Architectures using a Heterogeneous Interconnection Network". *Proc. of the 14th IEEE Int. Conference on High Performance Computing* (**HiPC**), Goa, India, ISBN: 3-540-77219-7. *Lecture Notes in Computer Science*, vol. 4873, Springer-Verlag, pp. 133-146, ISSN: 0302-9743, Dec. 2007

[C.32] J.M. Cebrián, J.L. Aragón, J.M. García and S. Kaxiras. "Adaptive VP Decay: Making Value Predictors Leakage-efficient Designs for High Performance Processors". *Proc. of the 4th ACM Int. Conference on Computing Frontiers* (**CF**), Ischia, Italy, pp. 113-122, ISBN: 978-1-59593-683-7, May 2007

[C.33] A. Flores, J.L. Aragón and M.E. Acacio. "Sim-PowerCMP: A Detailed Simulator for Energy Consumption Analysis in Future Embedded CMP Architectures". *Proc. of the 4th IEEE Int. Symposium on Embedded Computing* (**SEC**), Niagara Falls, Canada, pp. 752-757, ISBN: 0-7695-2847-3, May 2007

[C.34] J.M. Cebrián, J.L. Aragón and J.M. García. "Leakage Energy Reduction in Value Predictors through Static Decay". *Proc. of the Int. Workshop on High-Performance, Power-Aware Computing* (**HP-PAC**)*, in conjunction with IPDPS'2007*, Long Beach, CA (USA), pp. 269-275, ISBN: 1-4244-0909-8, March 2007

[C.35] J.L. Aragón and A. Veidenbaum. "Energy-Effective Instruction Fetch Unit for Wide Issue Processors". *Proc. of the 10th Asia-Pacific Computer Systems Architecture Conference* (**ACSAC**), Singapore, ISBN: 3-540-29643-3. *Lecture Notes in Computer Science*, vol. 3740, Springer-Verlag, pp. 15-27, ISSN: 0302-9743, October 2005

[C.36] J.L. Aragón, D. Nicolaescu, A. Veidenbaum and A.M. Badulescu. "Energy–Efficient Design for Highly Associative Instruction Caches in Next–Generation Embedded Processors". *Proc. of the IEEE Int. Conference on Design, Automation and Test in Europe* (**DATE**), Paris, France, pp. 1374-1375, ISBN: 0-7695-2085-5, Feb. 2004

[C.37] J.L. Aragón, J. González and A. González. "Power-Aware Control Speculation through Selective Throttling". *Proc. of the 9th IEEE Int. Symposium on High Performance Computer Architecture* (**HPCA**), Anaheim, CA (USA), pp. 103-112, ISBN: 0-7695-1871-0, Feb. 2003

[C.38] J.L. Aragón, J. González, A. González and J.E. Smith. "Dual Path Instruction Processing". *Proc. of the 16th ACM Int. Conference on Supercomputing* (**ICS**), New York, NY (USA), pp. 220-229, ISBN: 1-58113-483-5, June 2002

[C.39] J.L. Aragón, J. González, J.M. García and A. González. "Confidence Estimation for Branch Prediction Reversal". *Proc. of the 8th IEEE Int. Conference on High Performance Computing* (**HiPC**), Hyderabad (India), ISBN: 3-540-43009-1. *Lecture Notes in Computer Science*, vol. 2228, Springer-Verlag, pp. 214-223, ISSN: 0302-9743, Dec. 2001

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NATIONAL (SPANISH) CONFERENCES:

[C.41] A. Vicente-Jaén, J. Mompeán, J.L. Aragón and P. Artal. "cuElSe y cuExCuSe: seguimiento pupilar de alto rendimiento mediante GPUs". *Proc. of the XXXIV Jornadas de Paralelismo*, pp. 37-44, ISBN: 978-84-09-61749-4, A Coruña (Spain), June 2024

[C.42] A. Vicente-Jaén, J. Mompeán, J.L. Aragón and P. Artal. "GPU-accelerated Spatio-Temporal Reconstruction of OCT Volumes". *Proc. of the XXXIII Jornadas de Paralelismo*, pp. 323-329, ISBN: 978-84-09-54466-0, Ciudad Real (Spain), September 2023

[C.43] D. Corbalán-Navarro, J.L. Aragón, M. Anglada, E. de Lucas, J.M. Parcerisa and A. González. "Improving the Energy Efficiency of the Graphics Pipeline by Reducing Overshading". *Proc. of the XXXI Jornadas de Paralelismo*, pp. 125-134, ISBN: 978-84-09-32487-3, Málaga, September 2021

[C.44] J. Mompeán, J.L. Aragón, P. Prieto and P. Artal. "Cálculo de Mapas de Frentes de Onda mediante GPUs para Aplicaciones de Óptica Adaptativa en Tiempo Real". *Proc. of the XXVIII Jornadas de Paralelismo*, pp. 107-112, ISBN: 978-84-697-4835-0, Málaga (Spain), September 2017

[C.45] J. Mompeán, J.L. Aragón, P. Prieto and P. Artal. "Robust High-speed Eye Pupil Tracking System on GPUs". *Proc. of the XXVII Jornadas de Paralelismo*, pp. 47-52, ISBN: 978-84-9012-626-4, Salamanca (Spain), September 2016

[C.46] A. Flores, M.E. Acacio and J.L. Aragón. "Reducing the Energy Consumption of Hardware Prefetching in Many-Core CMPs using Reply Partitioning". *Proc. of the XXII Jornadas de Paralelismo*, pp. 227-232, ISBN: 978-84-694-1791-1, La Laguna (Spain), September 2011

[C.47] D. Sánchez, Y. Sazeides, J.L. Aragón and J.M. García. "Modelling Permanent Fault Impact on Cache Performance". *Proc. of the XXII Jornadas de Paralelismo*, pp. 233-238, ISBN: 978-84-694-1791-1, La Laguna (Spain), September 2011

[C.48] J.M. Cebrián, J.L. Aragón and S. Kaxiras. "Mechanisms to Match Power Constraints in CMPs". *Proc. of the XXI Jornadas de Paralelismo*, pp. 185-192, ISBN: 978-84-92812-49-3, Valencia (Spain), September 2010

[C.49] A. Flores, J.L. Aragón and M.E. Acacio. "Hardware Prefetching in Heterogeneous Interconnects: an Approach to Reducing Energy Consumption in Many-Core CMPs". *Proc. of the XXI Jornadas de Paralelismo*, pp. 177-184, ISBN: 978-84-92812-49-3, Valencia (Spain), September 2010

[C.50] J.M. Cebrián, J.L. Aragón, J.M. García, P. Petoumenos and S. Kaxiras. "Energy-Efficient Power Budget Matching". *Proc. of the XX Jornadas de Paralelismo*, pp. 195-200, ISBN: 84-9749-346-8, A Coruña (Spain), September 2009

[C.51] A. Flores, M.E. Acacio and J.L. Aragón. "Power-Aware On-Chip Network Management in Tiled CMPs using Address Compression". *Proc. of the XIX Jornadas de Paralelismo*, pp. 205-210, ISBN: 978-84-8021-676-0, Castellón (Spain), September 2008

[C.52] D. Sánchez, J.L. Aragón and J.M. García. "Adapting Dynamic Core Coupling to a Direct-Network Environment". *Proc. of the XIX Jornadas de Paralelismo*, pp. 253-258, ISBN: 978-84-8021-676-0, Castellón (Spain), September 2008

[C.53] J.M. Cebrián, J.L. Aragón, J.M. García and S. Kaxiras. "An Adaptive Approach for Reducing Leakage Energy Consumption in Value Predictors". *Proc. of the XVIII Jornadas de Paralelismo*, pp. 107-114, ISBN: 978-84-9732-593-6, Zaragoza (Spain), September 2007

[C.54] J.M. Cebrián, J.L. Aragón and J.M. García. "Reducing Leakage in Value Predictors by Using Decay Techniques". *Proc. of the XVII Jornadas de Paralelismo*, pp. 61-66, ISBN: 84-690-0551-0, Albacete (Spain), September 2006

[C.55] A. Flores, J.L. Aragón and M.E. Acacio. "Sim-PowerCMP: Un simulador de consumo para CMPs". *Proc. of the XVII Jornadas de Paralelismo*, pp. 85-90, ISBN: 84-690-0551-0, Albacete (Spain), September 2006

[C.56] J.L. Aragón and A. Veidenbaum. "Low-power Fetch Unit Design for Superscalar Processors". *Proc. of the XV Jornadas de Paralelismo*, pp. 173-178, ISBN: 84-8240-714-7, Almería (Spain), Sep. 2004

[C.57] J.L. Aragón, J. González, J.M. García and A. González. "Branch Prediction Reversal by Correlating with Data Values". *Proc. of the XII Jornadas de Paralelismo (XII Spanish Workshop on Parallelism)*, pp. 9-14, ISBN: 84-9705-043-6, Valencia (Spain), September 2001

OPTICS JOURNALS & CONFERENCES:

[Op.1] H. Hofer, P. Artal, J.L. Aragón and D.R. Williams. "Dynamics of the eye's wave aberration". *Journal of the Optical Society of America A*, 18(3), pp. 497-506, ISSN: 0740-3232, March 2001

[Op.2] J.L. Aragón, N. López-Gil and P. Artal. "Real-time double-pass system to study the dynamics of the eye's optical performance". *Proc. of the EOS Topical Meeting on Physiological Optics*, pp. 49-50, ISSN:1167-5357, Wroclaw (Poland), Sep. 1999

[Op.3] P. Artal, H.J. Hofer, D.R. Williams and J.L. Aragón. "Dynamics of ocular aberrations during accommodation". *Proc. of the OSA Annual Meeting*, California (USA), Sep. 1999

[Op.4] P. Artal, J.L. Aragón, P.M. Prieto, F. Vargas-Martín and E. Berrio. "Hartmann-Shack wavefront sensor in the eye: accuracy and performance limits". *Proc. of the Int. Workshop on Adaptive Optics for Industry and Medicine*, ISBN: 981-02-4115-1, Durham (England), July 1999

[Op.5] H.J. Hofer, P. Artal, J.L. Aragón and D.R. Williams. "Temporal characteristics of the eye's aberrations". *Journal of Inv. Ophth.Vis.Sci.*, Sppl. 40, 4, ISSN: 0146-0404, May 1999

PATENTS:

- *Title*: "Rapid, automatic measurement of the eye's wave aberration"
  Inventors: D.R. Williams, W.J. Vaughn, B.D. Singer, H. Hofer, G.Y. Yoon, P. Artal, J.L. Aragón, P. Prieto and F. Vargas
  - Patent #1 (US): **US 6199986 B1** (*Granted* Mar. 13th, 2001)
  - Extension #2 (US): **US 6827444 B2** (*Granted* Dec. 7th, 2004)
  - Extension #3 (Singapore): **SP 88309** (*Granted* June 30th, 2005)
  - Extension #4 (Japan): **JP 4660047 B2** (*Granted* Mar. 30th, 2011)
- *Title*: "Instrumento Binocular Optoelectrónico para la Corrección de la Presbicia y Método para la Corrección Binocular de la Presbicia"
  Inventors: P. Artal, J. Mompeán and J.L. Aragón
  - Patent #1 (Spain): **ES 2659087 B1** (*Granted* Jan. 15th, 2019)
- *Title*: "Optoelectronic binocular instrument for the correction of presbyopia and method for the binocular correction of presbyopia"
  Inventors: P. Artal, J. Mompeán and J.L. Aragón
  - Patent #1 (US): **US 10898073 B2** (*Granted* Jan. 26th, 2021, *Published* 13/06/2019)
  - Extension #2 (Europe): **EP 3498149 B1** (*Granted* August 2nd, 2023, *Published* 19/06/2019)
  - Extension #3 (China): **CN 109803573 A** (*Published* May 24th, 2019)

RESEARCH PROJECTS PARTICIPATION

1. *Project*: "Design of Energy-Sustainable and Efficient Computing Systems"
   Principal Investigator: Juan L. Aragón, UMU, Spain
   Granted by: Spanish MICINN, TED2021-130233B-C33, years 2023-2024
2. *Project*: "Development of Advanced Techniques for Improving the Architecture of Superchips"
   Principal Investigator: Manuel E. Acacio, UMU, Spain
   Granted by: Spanish MICINN, PID2022-136315OB-I00, years 2023-2027
3. *Project*: "Desarrollo de gafas con lentes electro-ópticas"
   Principal Investigator: Pablo Artal, UMU, Spain
   Granted by: Spanish MICINN, CPP2022-009992, years 2023-2026
4. *Project*: "Domain-Specific Architectures for Energy-Efficient Computing Systems"
   Principal Investigator: Antonio González, UPC, Spain
   Granted by: Spanish MICINN, PID2020-113172RB-I00, years 2021-2025
5. *Project*: "Smart Glasses for Correction of Eye's Aberrations"
   Principal Investigator: Pablo Artal, UMU, Spain
   Granted by: Fundación "la Caixa", CaixaResearch Consolidate, LCF/TR/CC21/52490004, 2022-2023
6. *Project*: "Gafas Optoelectrónicas para la Corrección Automática de la Presbicia"
   Principal Investigator: Pablo Artal, UMU, Spain
   Granted by: Spanish MICINN, PDC2021-121575-I00, years 2021-2023

7. *Project*: “Técnicas Innovadoras en Computación Especializada y de Altas Prestaciones”
   Main Coordinator: José Duato, UPV, Spain
   Granted by: Spanish MICINN, RTI2018-098156-B-C53, years 2019-2021

8. *Project*: “Arquitectura de Sistemas de Computación Inteligentes, Ubicuos y Energéticamente Eficientes”
   Principal Investigator: Antonio González, UPC, Spain
   Granted by: Spanish MINECO, TIN2016-75344-R, years 2017-2020

9. *Project*: “Técnicas para la Mejora de las Prestaciones, Fiabilidad y Consumo de Energía de los Servidores. Optimización de Aplicaciones Científicas, Médicas y de Visión Artificial”
   Main Coordinator: José Duato, UPV, Spain
   Granted by: Spanish MINECO, TIN2015-66972-C5-3-R, years 2016-2018

10. *Project*: “Microarquitectura y Compiladores para Futuros Procesadores III”
    Principal Investigator: Antonio González, UPC, Spain
    Granted by: Spanish MINECO, TIN2013-44375-R, years 2014-2016

11. *Project*: “Mejora de Arquitectura de Servidores, Servicios y Aplicaciones”
    Main Coordinator: José Duato, UPV, Spain
    Granted by: Spanish MEC, TIN2012-38341-C04-03, years 2013-2015

12. *Project*: “Diseño de una Infraestructura Hardware para la Comunicación y Sincronización Eficientes en Arquitecturas Multicore para Servidores”
    Principal Investigator: Manuel E. Acacio, UMU, Spain
    Granted by: Fundación Séneca, Región de Murcia, 19295/PI/14, years 2015-2016

13. *Project*: “Arquitecturas de Servidores, Aplicaciones y Servicios”
    Main Coordinator: José Duato, UPV, Spain
    Granted by: Spanish MEC, TIN2009-14475-C04-02, years 2010-2012

14. *Project*: “Diseño de Arquitecturas CMP Eficientes Energéticamente y Fiables para Sistemas Empotrados de Próxima Generación”
    Principal Investigator: José M. García, UMU, Spain
    Granted by: Fundación Séneca, Región de Murcia, 05831/PI/07, years 2007-2009

15. *Project*: “Arquitecturas Fiables y de Altas Prestaciones para Centros de Proceso de Datos y Servidores de Internet”
    Main Coordinator: José Duato, UPV, Spain
    Granted by: Spanish MEC – Prog. Consolider-Ingenio 2010, CSD2006-00046, years 2006-2011

16. *Project*: “Mejora de las prestaciones, servicios y aplicaciones ofrecidas por arquitecturas cluster de altas prestaciones”
    Main Coordinator: José Duato, UPV, Spain
    Granted by: Spanish MEC, TIN2006-15516-C04-03, years 2006-2007

17. *Project*: “Mejora de las prestaciones y servicios ofrecidos por los clusters de computadores personales. Desarrollo de aplicaciones multimedia distribuidas II”
    Main Coordinator: José Duato, UPV, Spain
    Granted by: Spanish CICYT, TIC2003-08154-C06-03, years 2003-2006

18. *Project*: “Mejora de las prestaciones y servicios ofrecidos por las redes de computadores personales. Desarrollo de aplicaciones multimedia distribuidas”
    Main Coordinator: José Duato, UPV, Spain
    Granted by: Spanish CICYT, TIC2000-1151-C07-03, years 2001-2003

19. *Project*: "Estudios fundamentales en óptica fisiológica: óptica adaptativa, polarización, acomodación y modelización"
Principal Investigator: Pablo Artal, UMU, Spain
Granted by: Spanish CICYT, PB97-1056, years 1998-2001

20. *Project*: "Contact Lenses with Aspheric Asymetric Surfaces"
Principal Investigator: Pablo Artal, UMU, Spain
Granted by: European Union, FP4 BRPR-CT-98-0681, years 1998-2002

Ph.D. STUDENTS *(in chronological order)*

1. Antonio Flores (Associate Professor at the University of Murcia, Spain)
Title: "Improving the Performance and Reducing the Consumption of Multicore Processors using Heterogeneous Networks"
Advisors: Juan L. Aragón and Manuel E. Acacio (UMU, Spain)
Graduation: September 24th, 2010
Qualification: Summa cum laude

2. Daniel Sánchez-Pedreño (first job at Intel Barcelona Research Center - Intel Labs)
Title: "Microarchitectural Approaches for Hardware Fault Mitigation in Multicore Processors"
Advisors: Juan L. Aragón and José M. García (UMU, Spain)
Graduation: July 25th, 2011
Qualification: Summa cum laude

3. Juan M. Cebrián (first job as postdoc at Norwegian University of Science and Technology - NTNU)
Title: "Efficient Power and Thermal Management using Fine-grain Architectural Approaches in Multicores"
Advisors: Juan L. Aragón and Stefanos Kaxiras (Uppsala University)
Graduation: September 5th, 2011
Qualification: Summa cum laude

4. Tae Jun Ham (first job as postdoc at Seoul National University)
Title: "Data Access Optimization in Accelerator-Oriented Heterogeneous Architecture through Decoupling and Memory Hierarchy Specialization"
Advisors: Juan L. Aragón and Margaret Martonosi (Princeton University, USA)
Graduation: May 21st, 2018
Qualification: Summa cum laude

5. Juan Mompeán (first job as postdoc at the LOUM, University of Murcia)
Title: "Design of real-time systems through graphics and specialized accelerators for improving the human eye's vision"
Advisors: Juan L. Aragón and Pablo Artal (UMU, Spain)
Graduation: January 15th, 2021
Qualification: Summa cum laude

6. David Corbalán (first job at VOPTICA)
Title: "Design of energy-efficient GPUs by exploiting frame coherence and optimizing memory accesses"
Advisors: Juan L. Aragón and Antonio González (UPC, Spain)
Graduation: June 26th, 2023
Qualification: Summa cum laude

7. Diya Joseph (first job at Huawei)
   Title: "Improving Memory Access Efficiency for Real-time Rendering in Tile-based GPU Architectures"
   Advisors: Juan L. Aragón and Antonio González (UPC, Spain)
   Graduation: July 26th, 2024
   Qualification: Summa cum laude

8. Aurora Tomás (ongoing PhD student)
   Research line: "Microarchitecture-level Techniques for Parallel Tile Rendering on Mobile GPUs"
   Advisors: Juan L. Aragón and Antonio González (UPC, Spain)
   Graduation: in progress – 2nd year PhD student

9. Arturo Vicente-Jaén (ongoing PhD student)
   Research line: "Design of real-time systems using accelerators and deep learning techniques applied to human visual optics"
   Advisors: Juan L. Aragón and Pablo Artal (UMU, Spain)
   Graduation: in progress – 1st year PhD student

OTHER ACTIVITIES

- Program Committee member: EUROMICRO-PDP-2009, ISLPED-2010, EUROMICRO-PDP-2010, PDP-2011, PDP-2012, PDP-2013, PDP-2014, PDP-2015, PDP-2016, PDP-2017, PDP-2018, PDP-2019, PDP-2020, PDP-2021, PDP-2022, HPCA-2022, HPCA-2023, MICRO-2023
- Workshop Chair: ISCA 2017
- Conference reviewer for: ISCA-2001, PDP-2002, ICCD-2002, HPCA-2003, ISCA-2003, ICS-2003, IWIA-2003, ESTImedia-2003, HPCA-2004, ACSAC-2004, PACT-2004, ICCD-2004, MICRO-2004, ICPP-2005, HiPC-2005, ISCA-2006, CASES-2007, PDP-2009, IPDPS-2009, Hot Interconnects-2009, HPCA-2010, PDP-2010, ISLPED-2010, PDP-2011, HPCA-2011, PDP-2012, ISLPED-2012, PDP-2013, PDP-2014, PDP-2015, HPCA-2015, ISCA-2015, PDP-2016, CGO-2016, ISCA-2016, HPCA-2016, PDP-2017, HPCA-2017, ISCA-2017, HPCA-2018, PDP-2018, MICRO-2018, PDP-2019, HPCA-2019, MICRO-2019, PDP-2020, HPCA-2020, PDP-2021, PDP-2022, HPCA-2022, HPCA-2023, MICRO-2023
- Journal reviewer for: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2024) / Journal of Supercomputing (2018, 2021) / IEEE Transactions on Computers (2002, 2005, 2006, 2007, 2013) / IEEE Transactions on Parallel and Distributed Systems (2011, 2012, 2013, 2016) / IEEE Computer Architecture Letters (2010, 2013, 2015) / ACM Transactions on Architecture and Code Optimization (2013) / IEEE Transactions on Very Large Scale Integration Systems (2009) / Journal of Systems Architecture (2003, 2005) / IEEE Computer (2007, 2009) / LNCS Transactions on HiPEAC (2007) / IEE Computers and Digital Techniques Journal (2003, 2004) / Journal of Computer Science and Technology (2006) / EURASIP Journal on Embedded Systems (2007) / IET Circuits, Devices & Systems (2012)