ALTERNATE PATH μ-OP CACHE PREFETCHING

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H2P Branch

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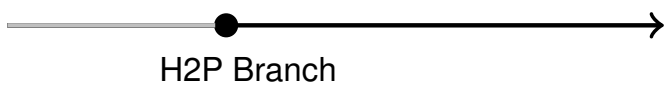

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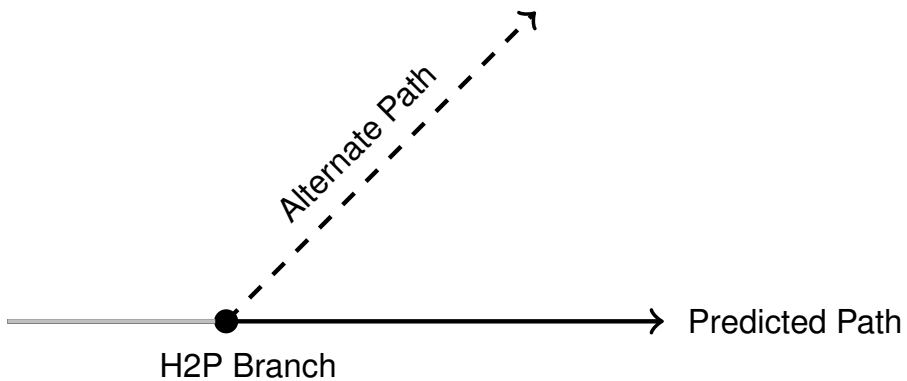

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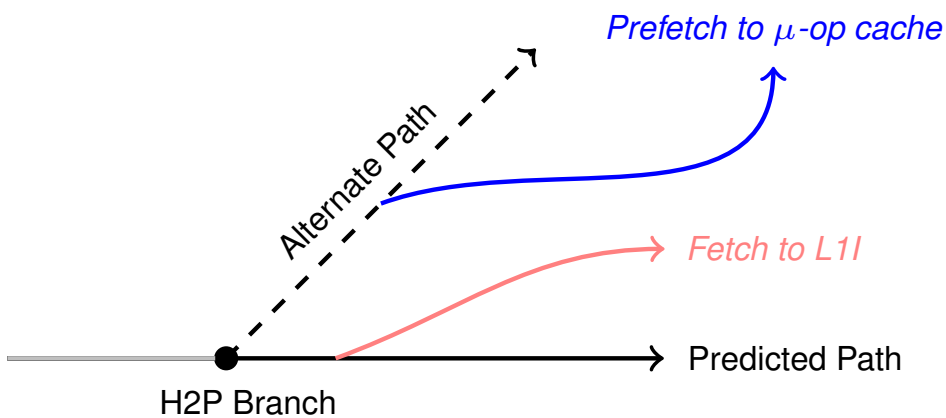

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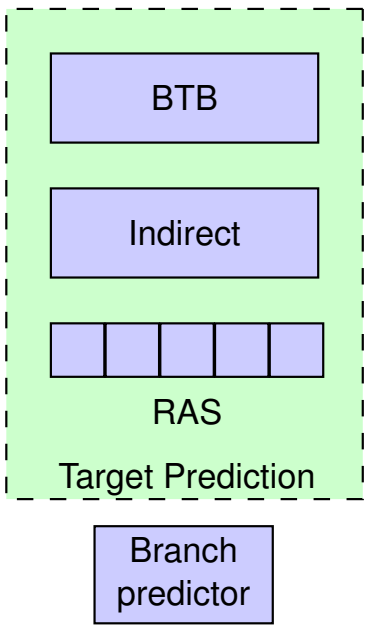
Outline

Background & Motivation

Processor Front-End



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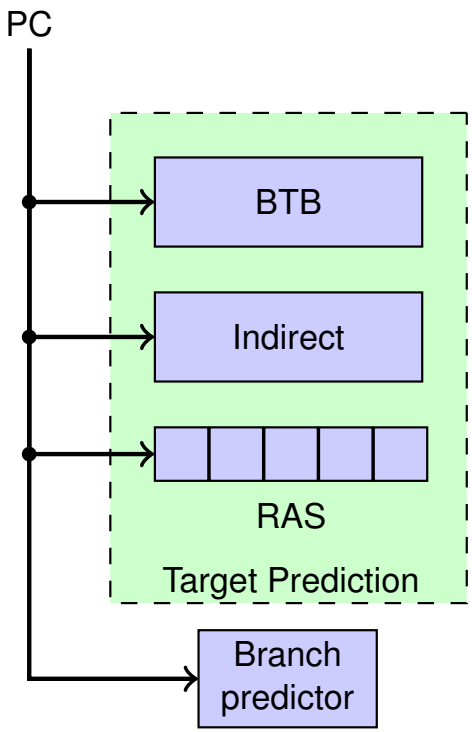

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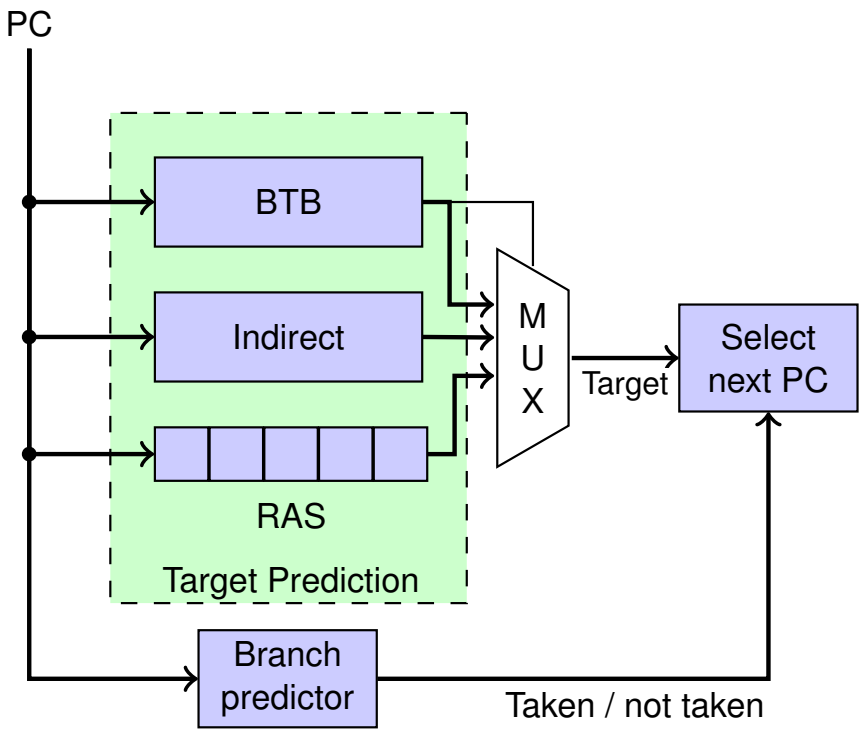

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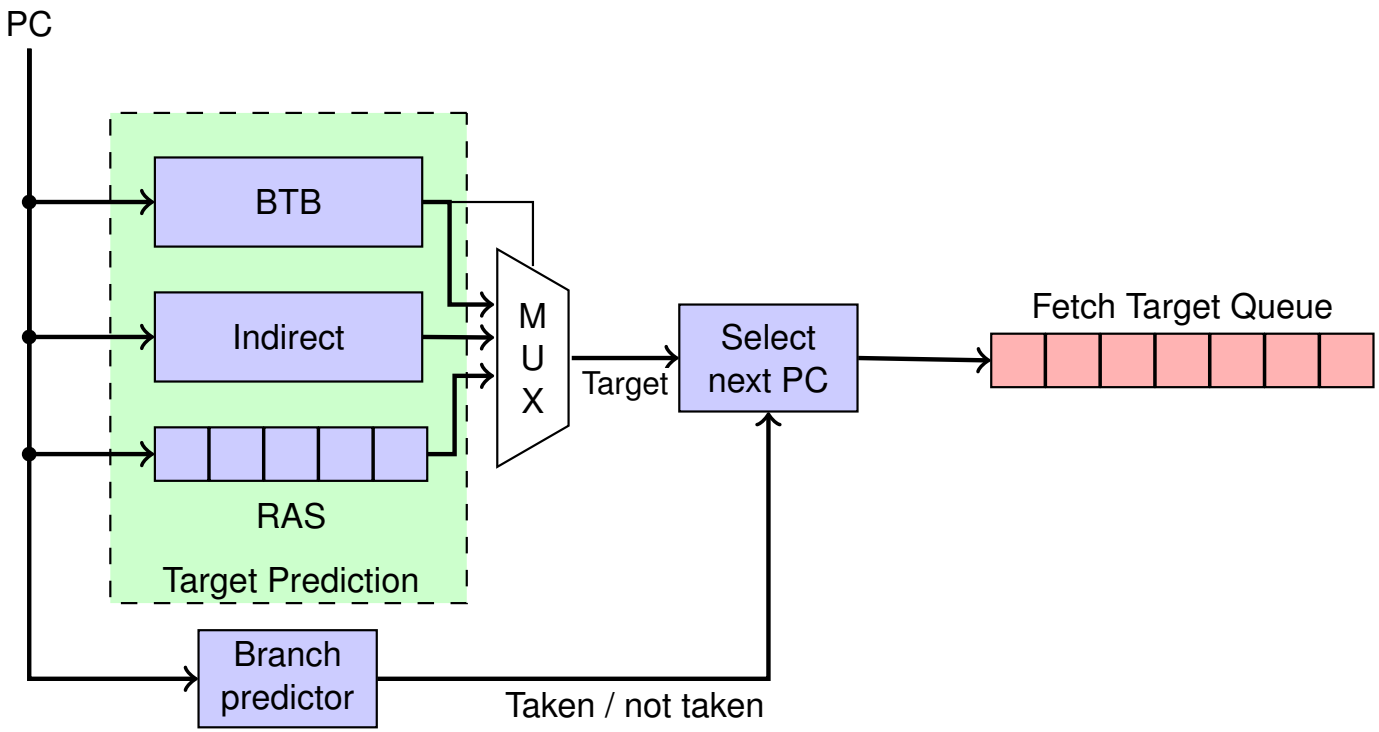

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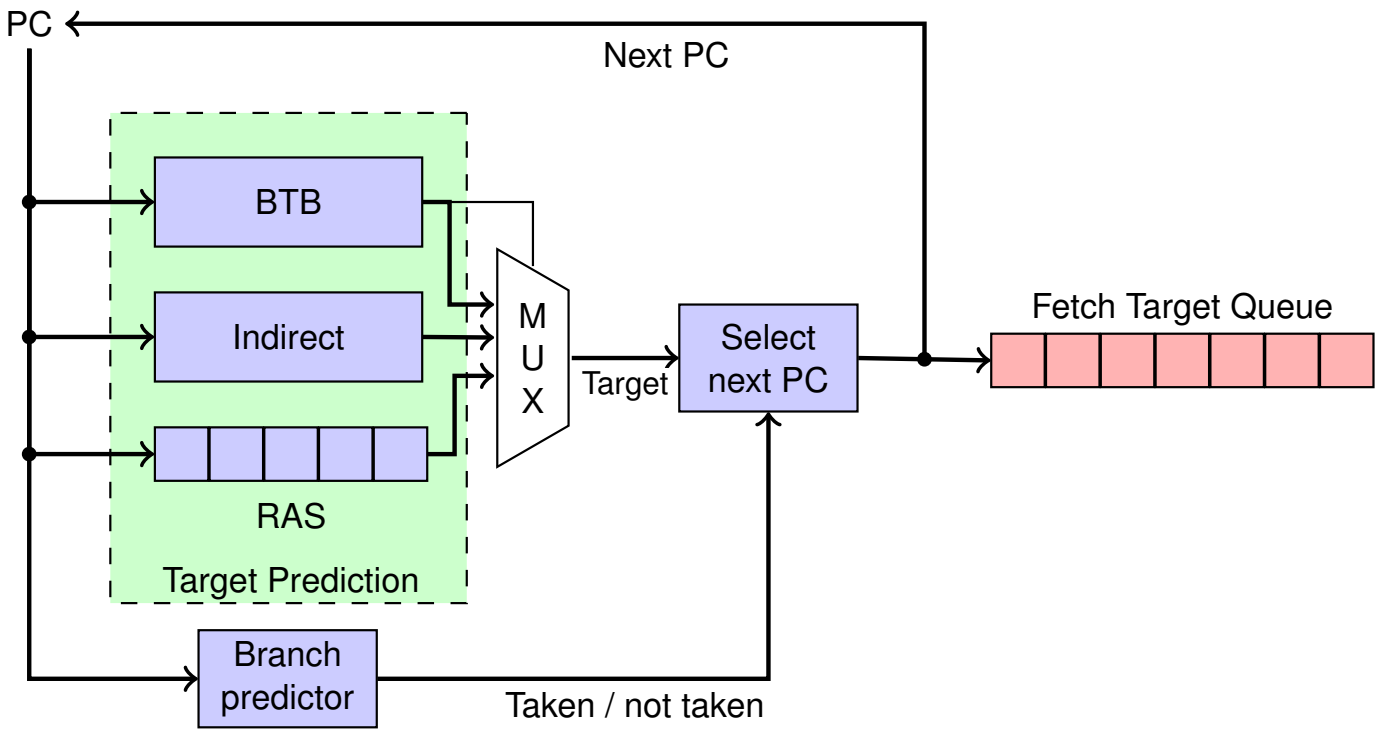

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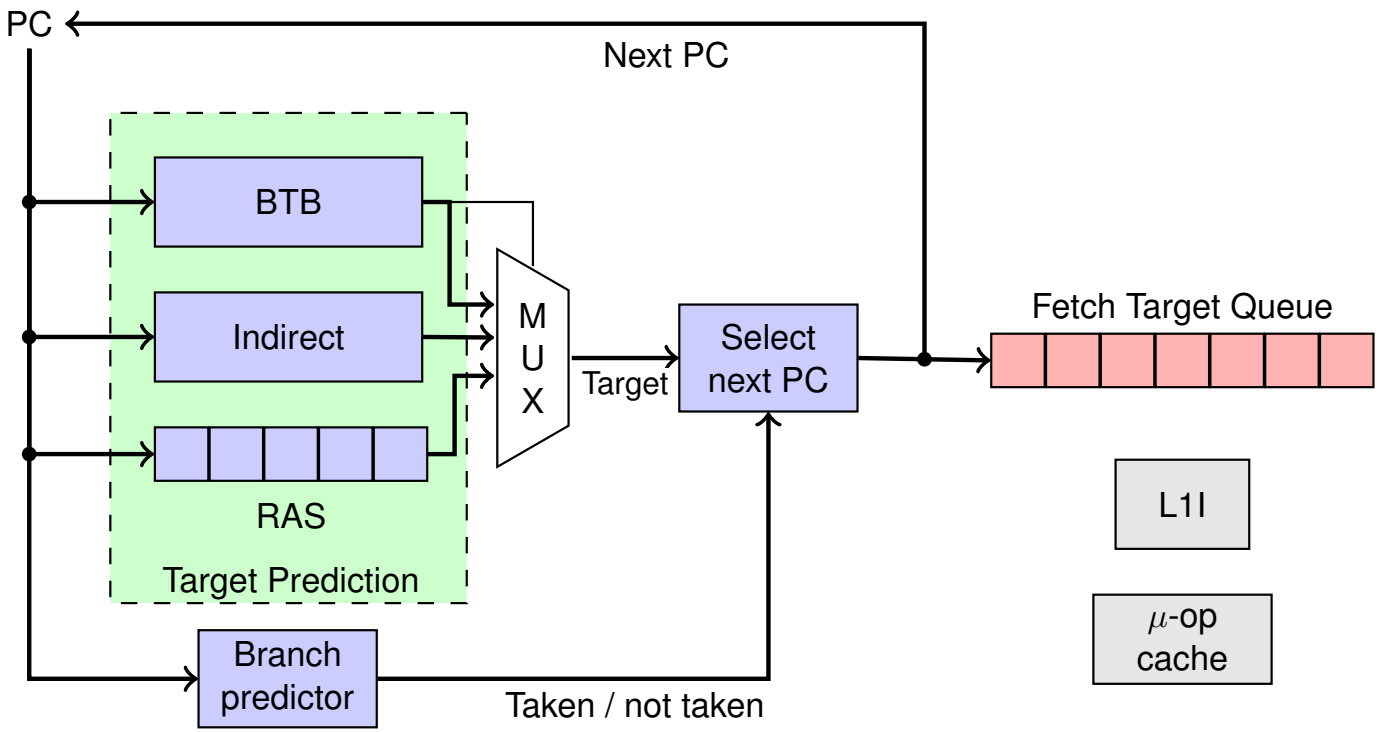

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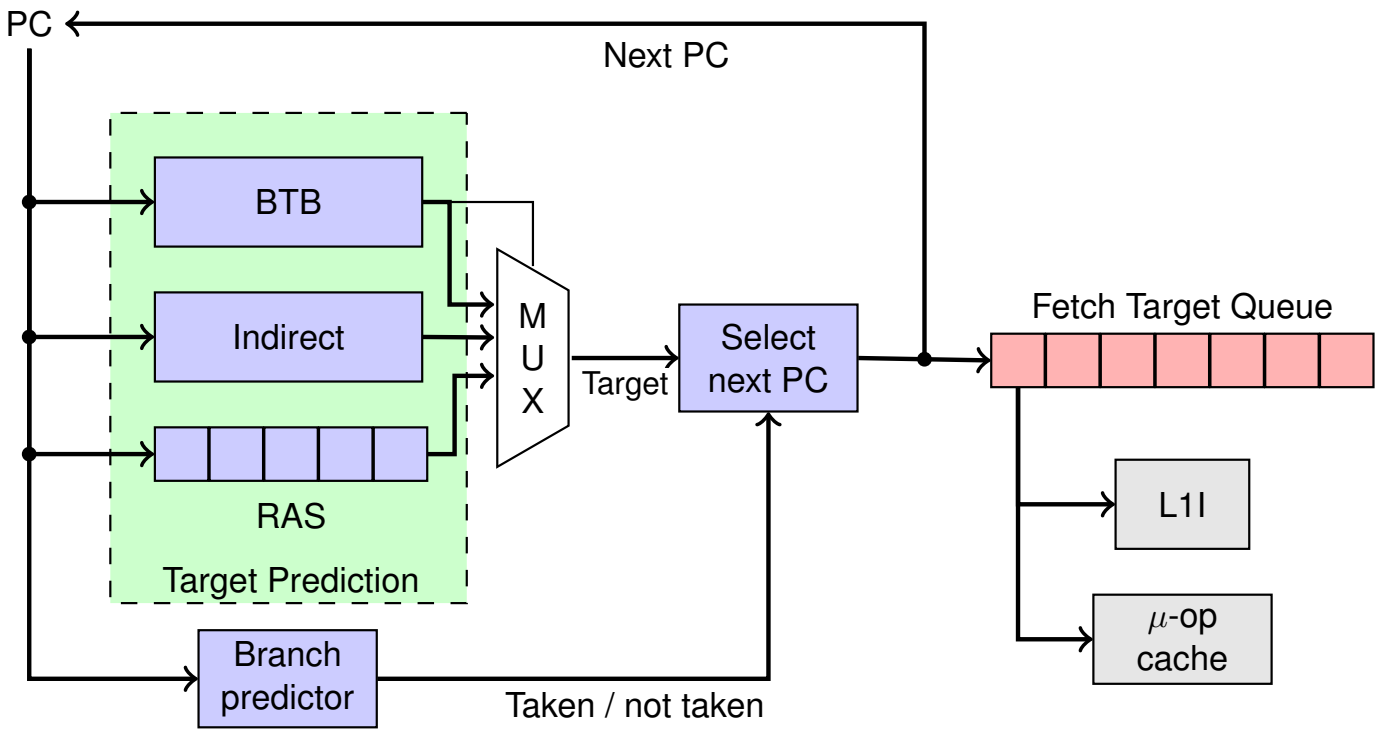

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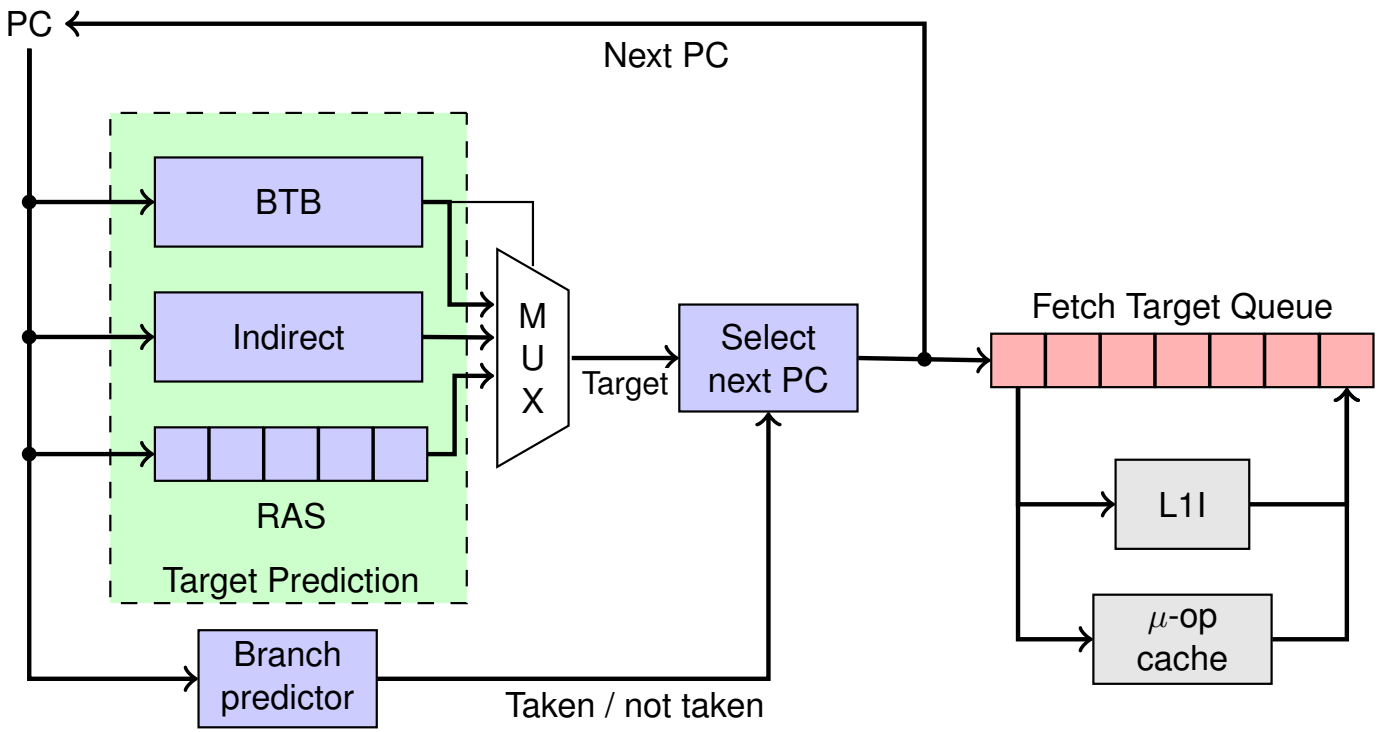

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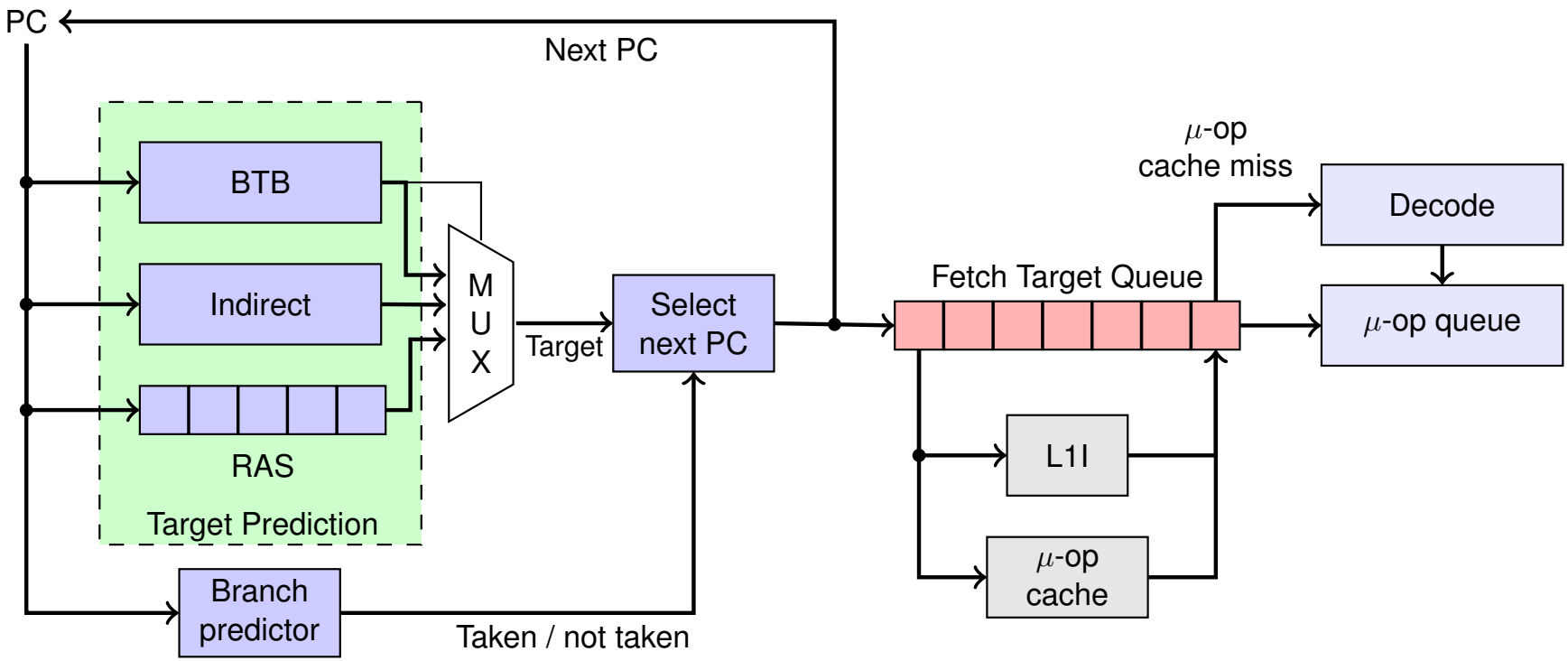

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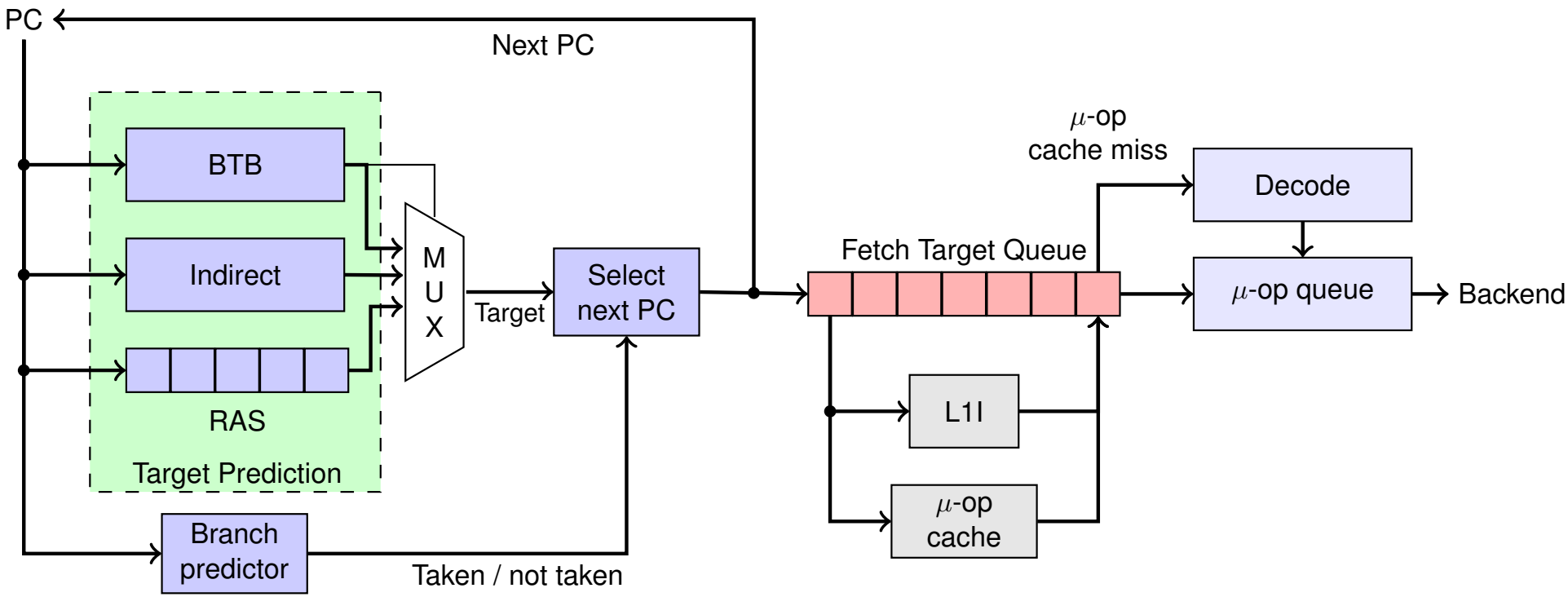


Background & Motivation

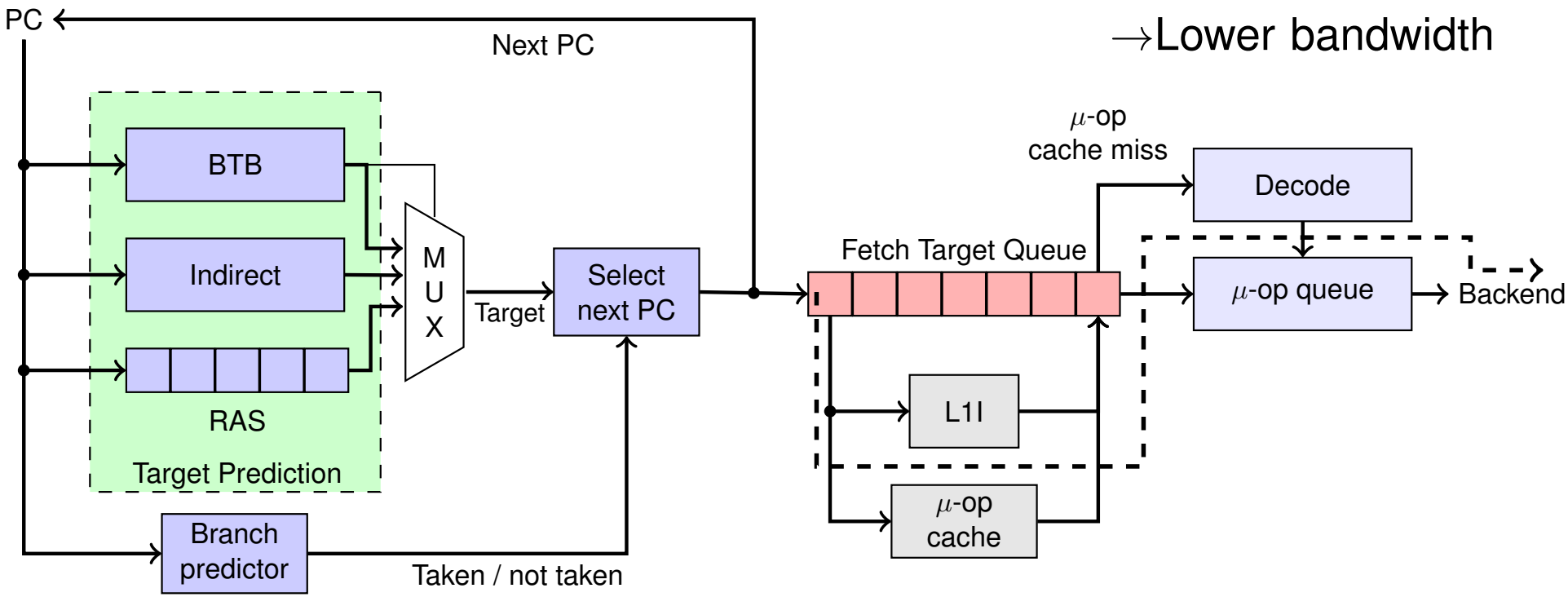
Processor Front-End

From L1I:

→Decode latency

→Decode energy

→Lower bandwidth



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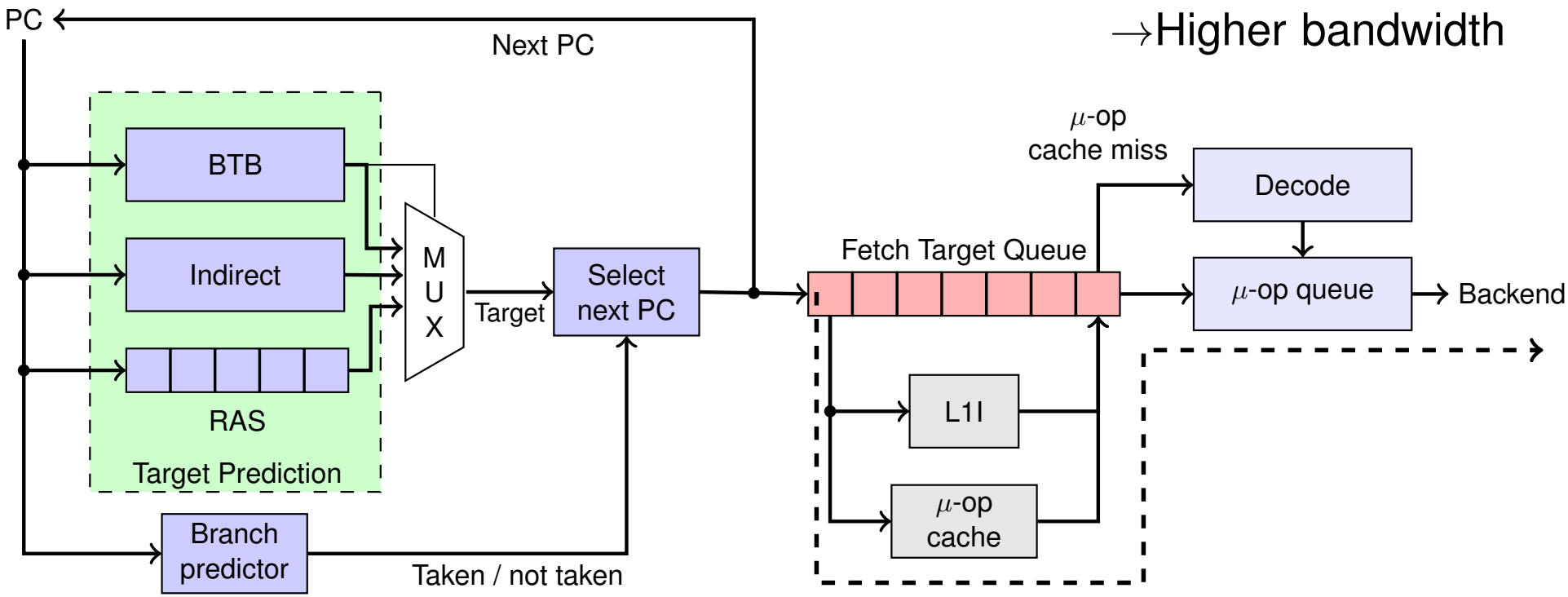
Processor Front-End

From μ-op cache:
- →~~Decode latency~~
- →~~Decode energy~~
- →Higher bandwidth



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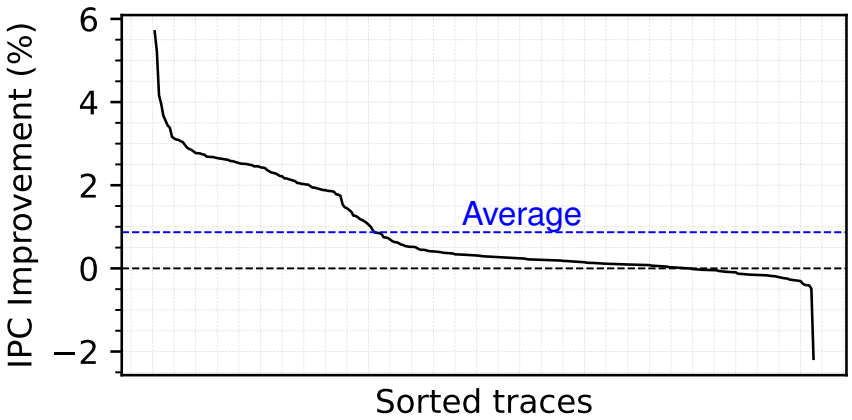
Performance of μ-ops cache with server workloads



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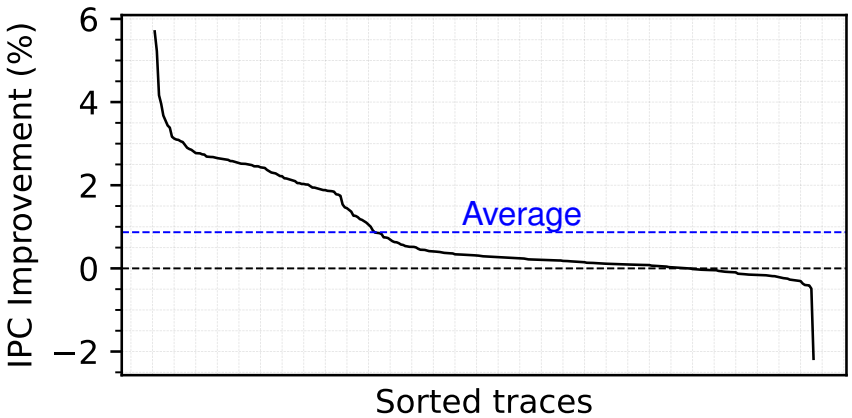

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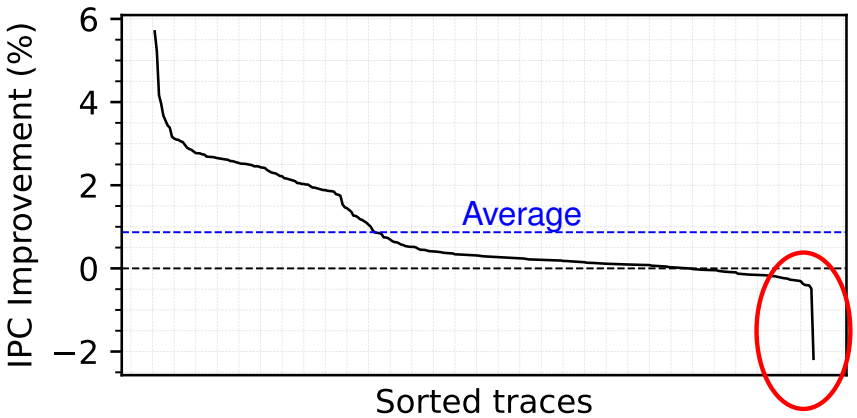

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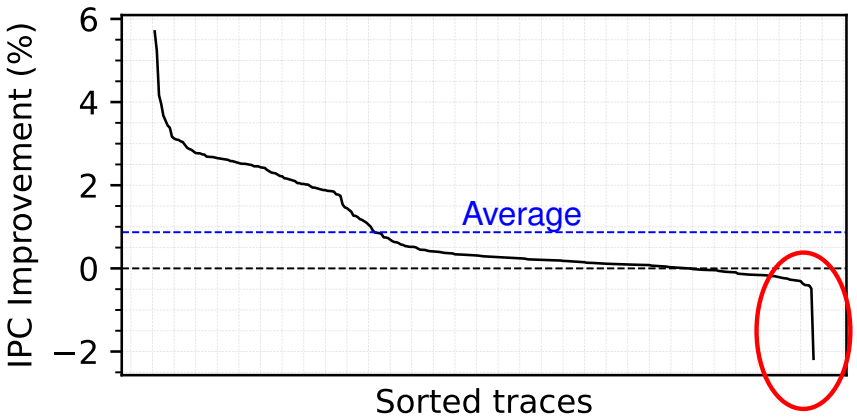

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IPC Improvement (w.r.t 4Kops μ-op cache) →

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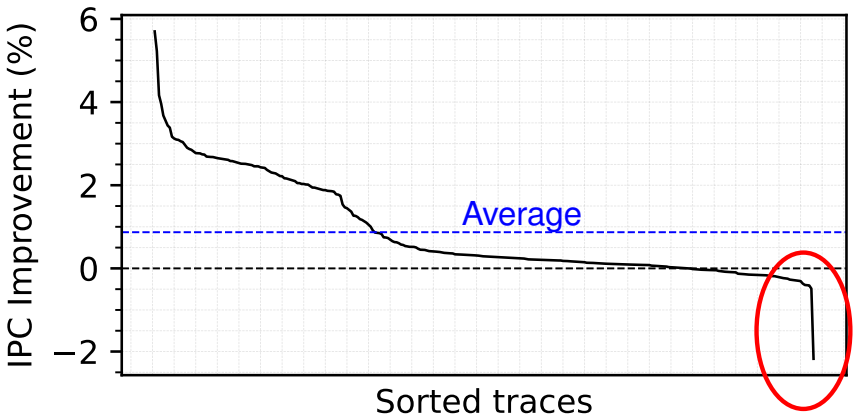

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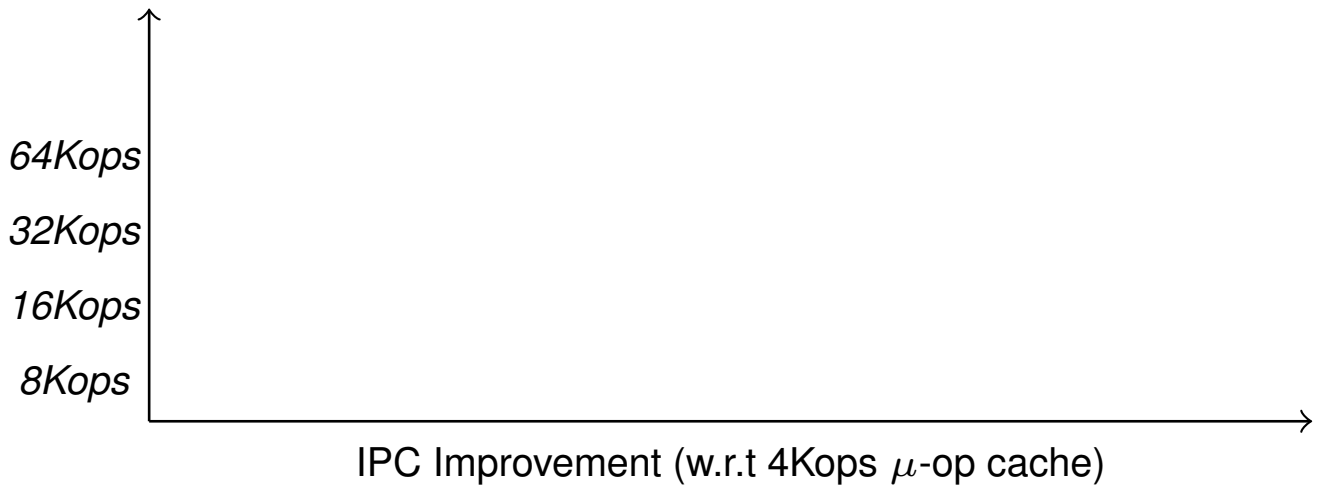

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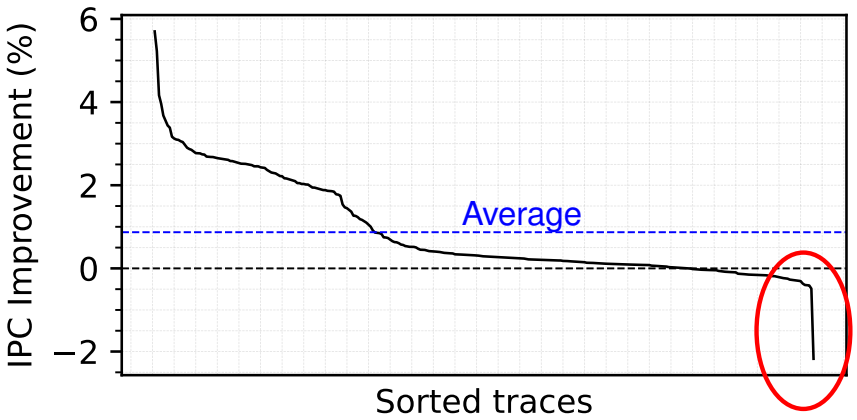

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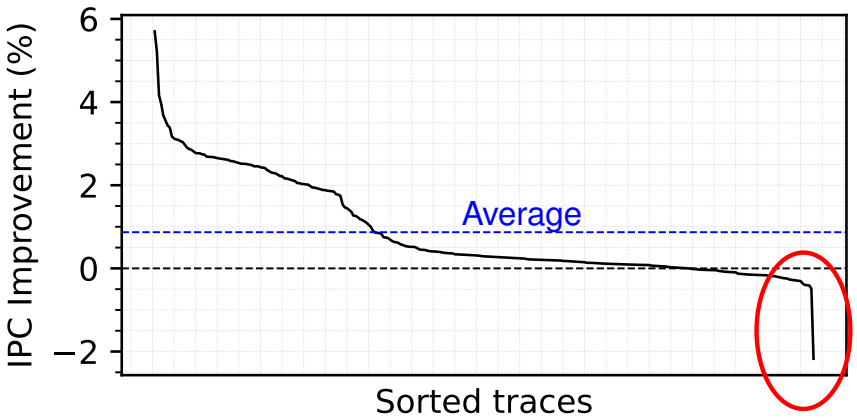

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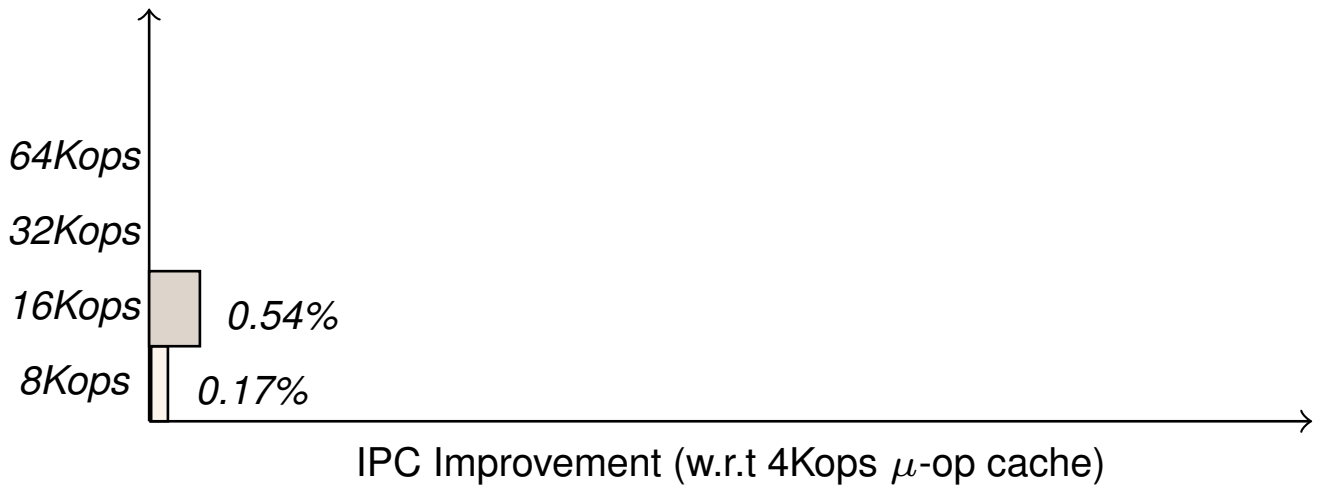

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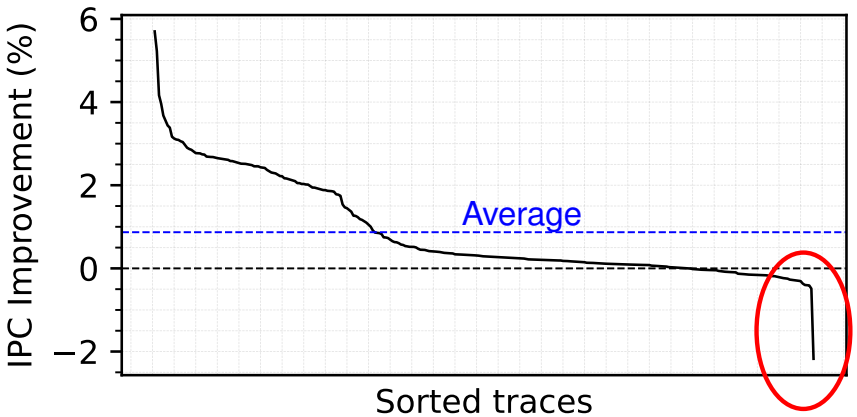

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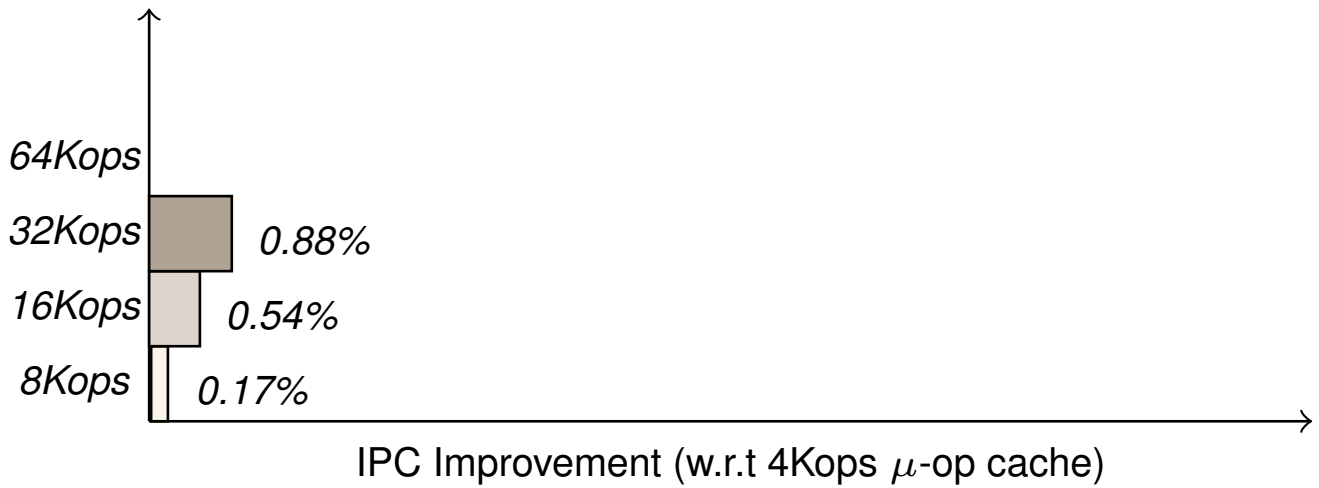

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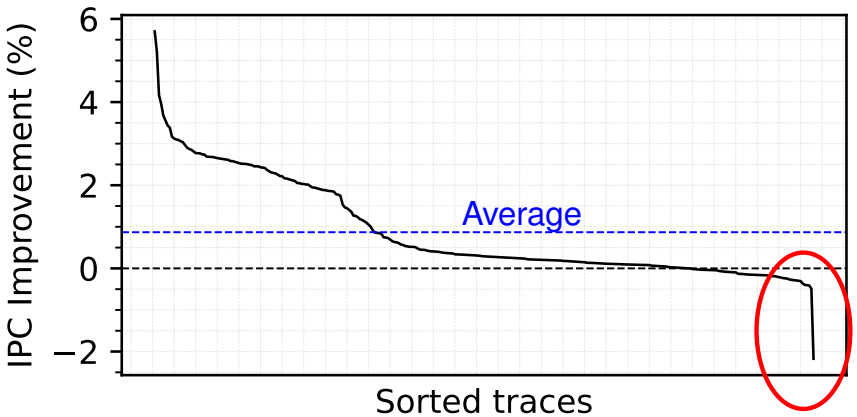

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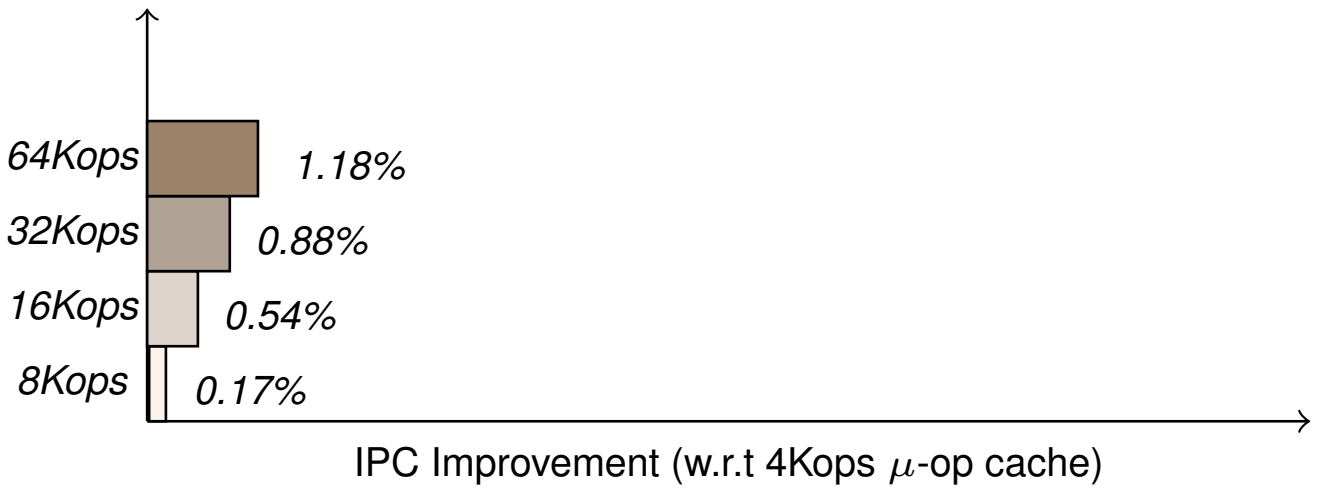

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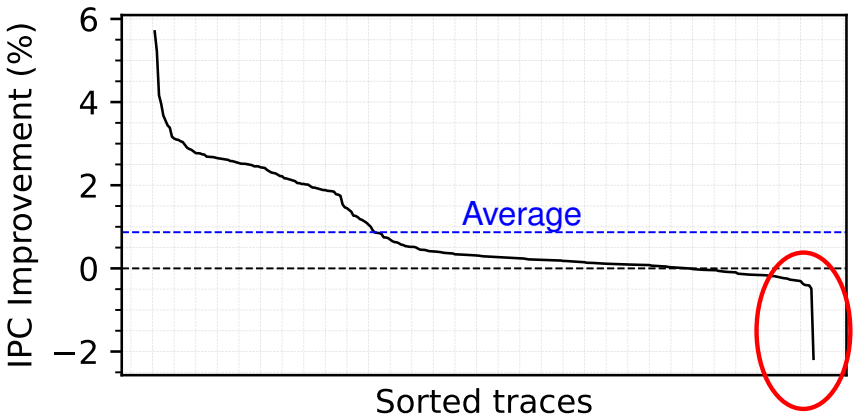

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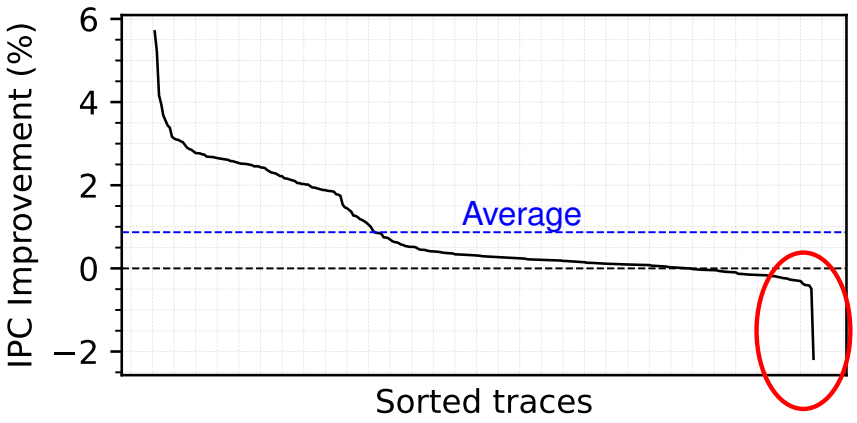

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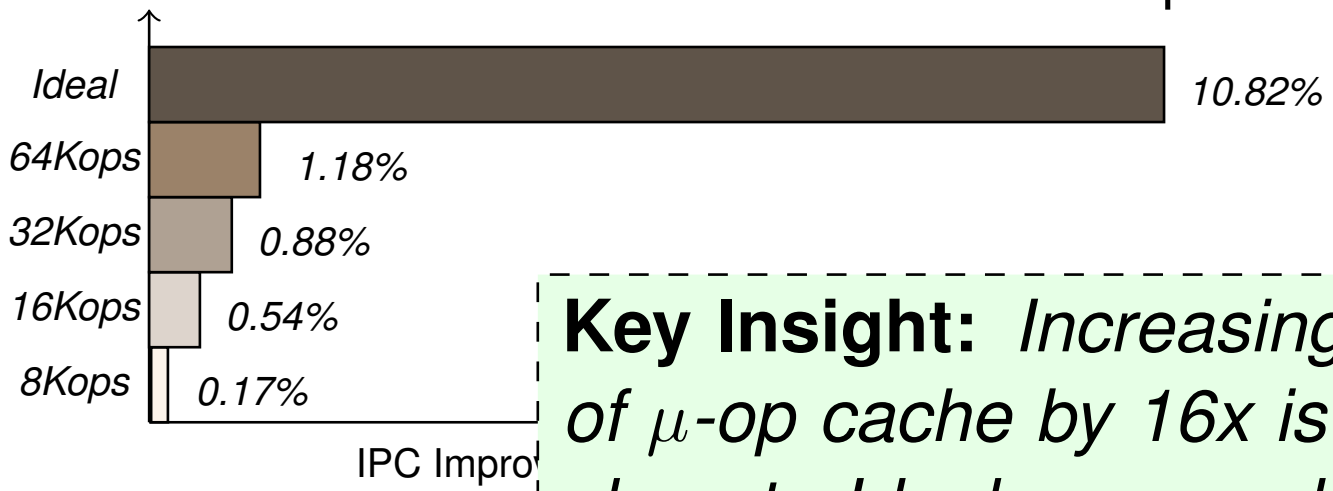

Key Insight: *Increasing the size of μ-op cache by 16x is still not close to Ideal μ-op cache*

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FTQ behavior on branch miss

→ FTQ is unable to hide the L1I miss latency on branch misprediction

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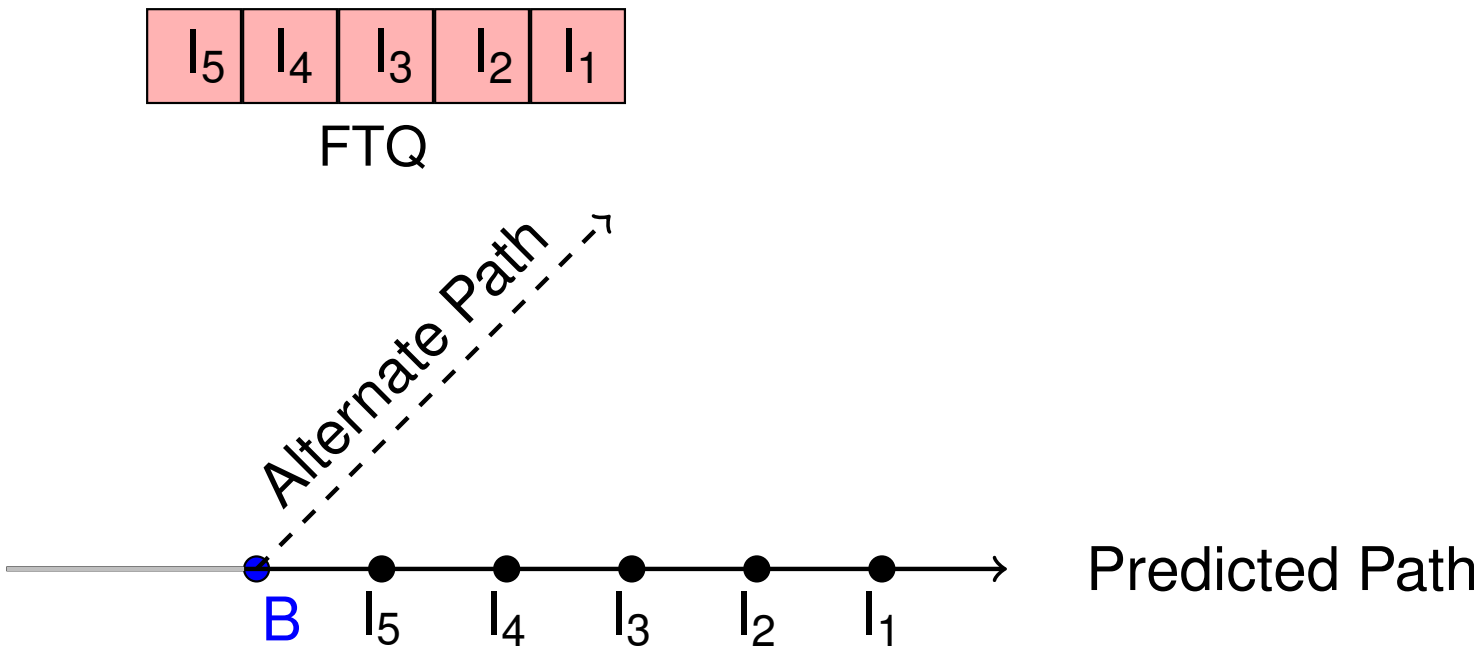

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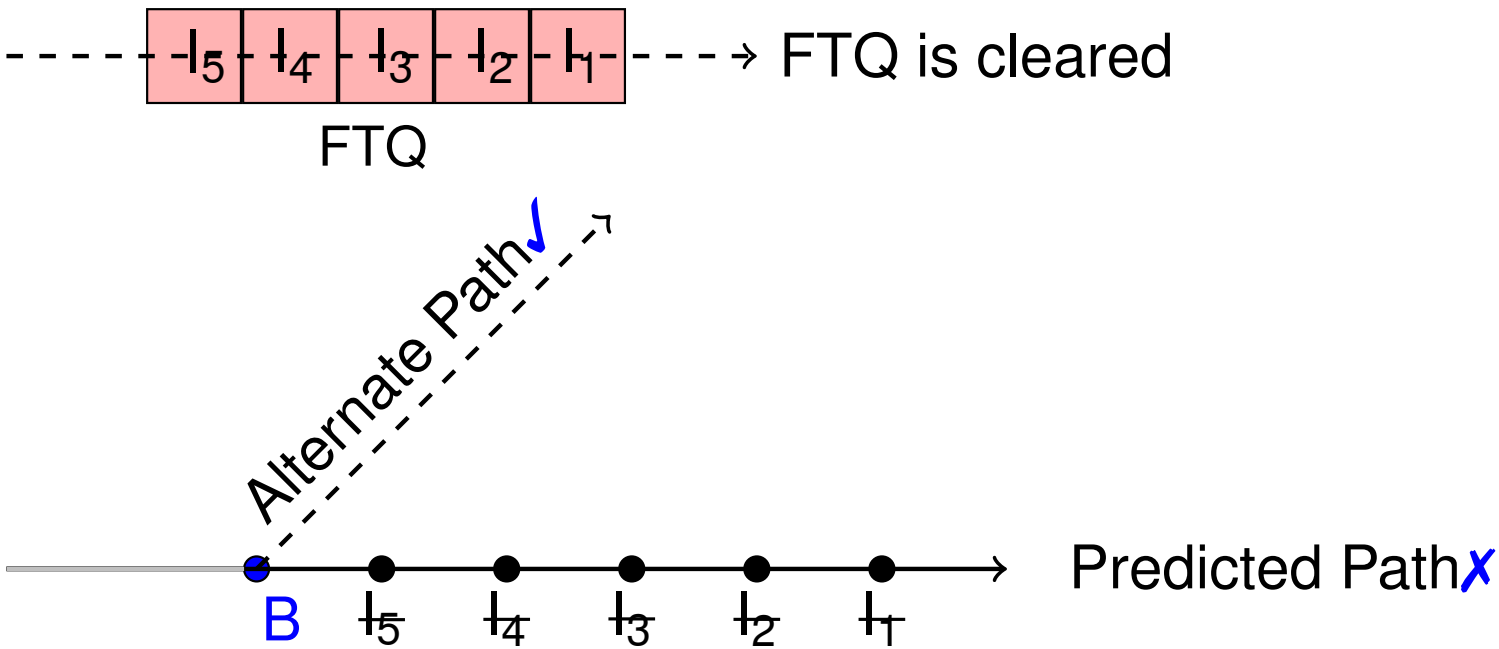

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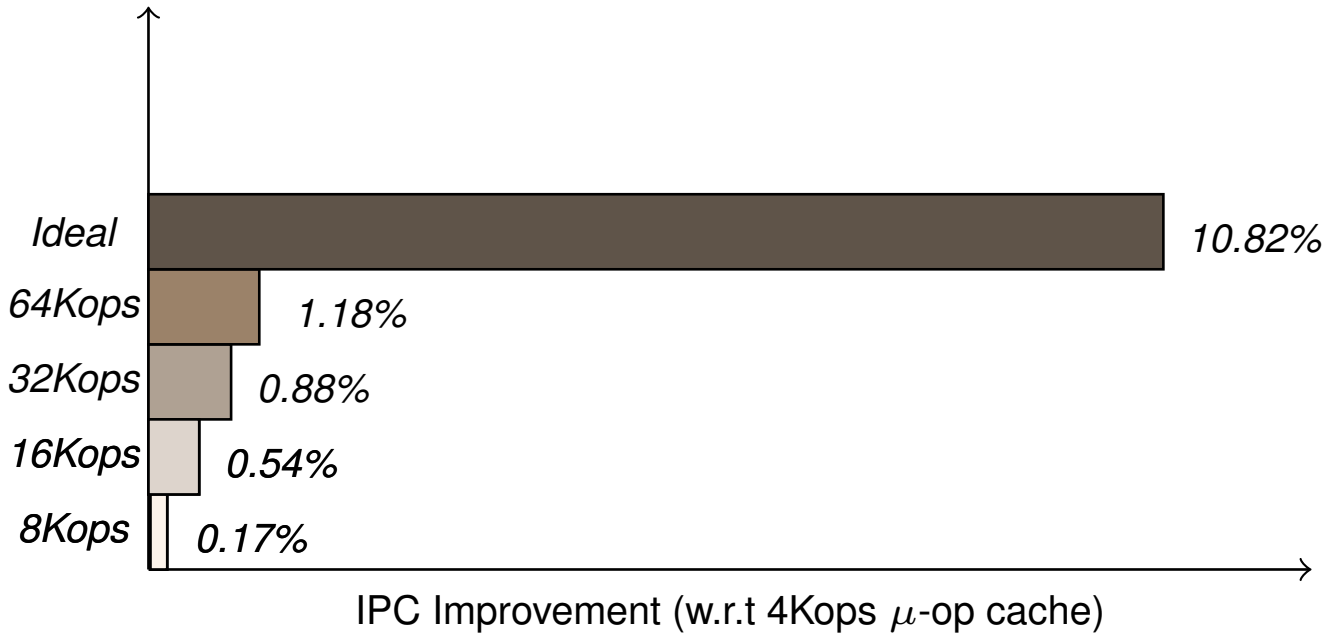

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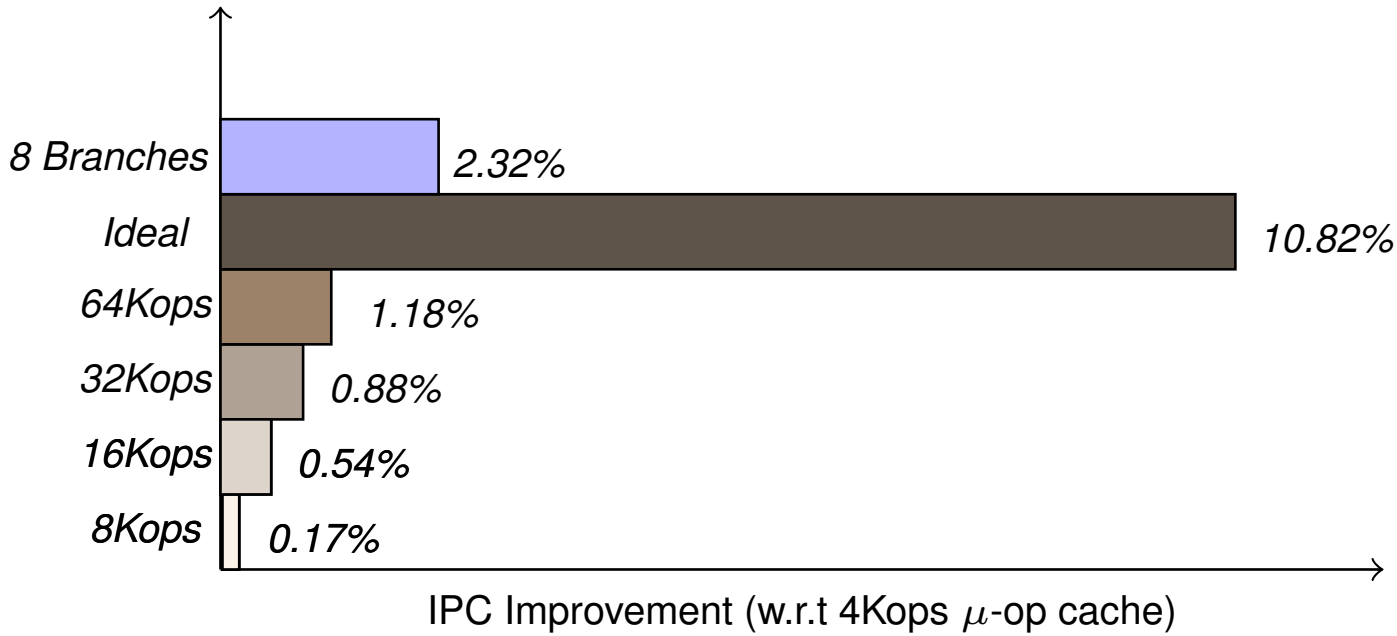

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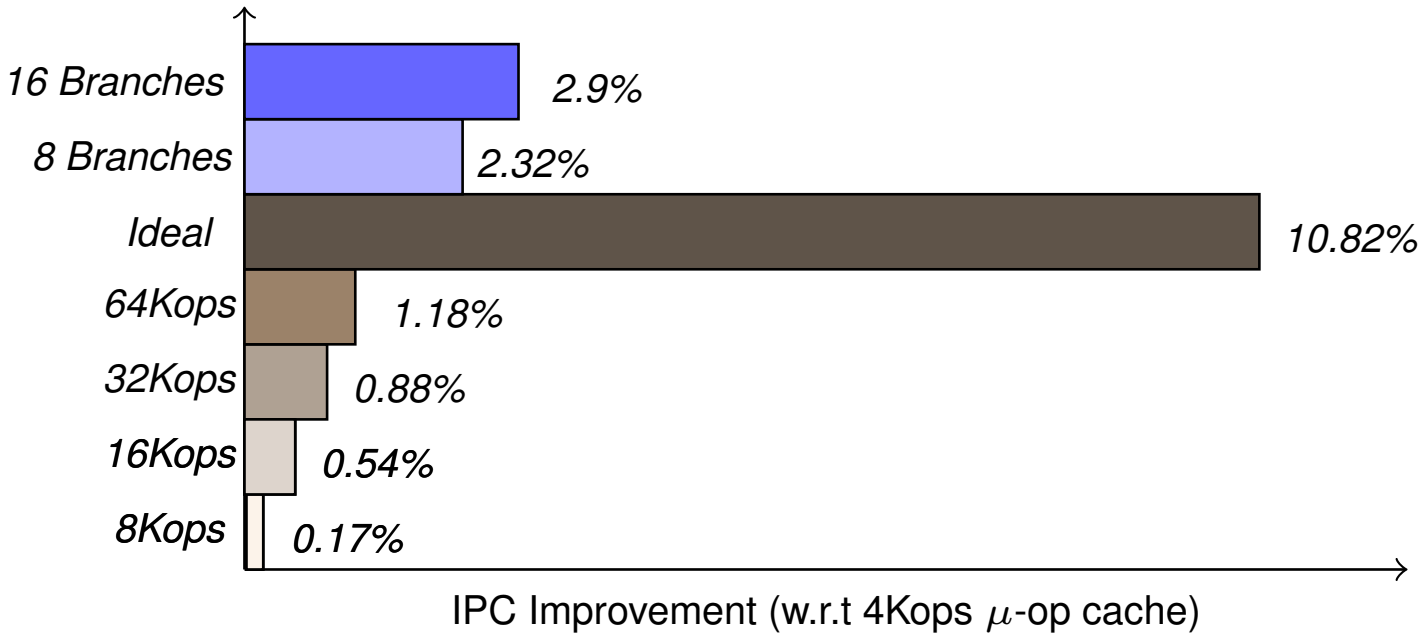

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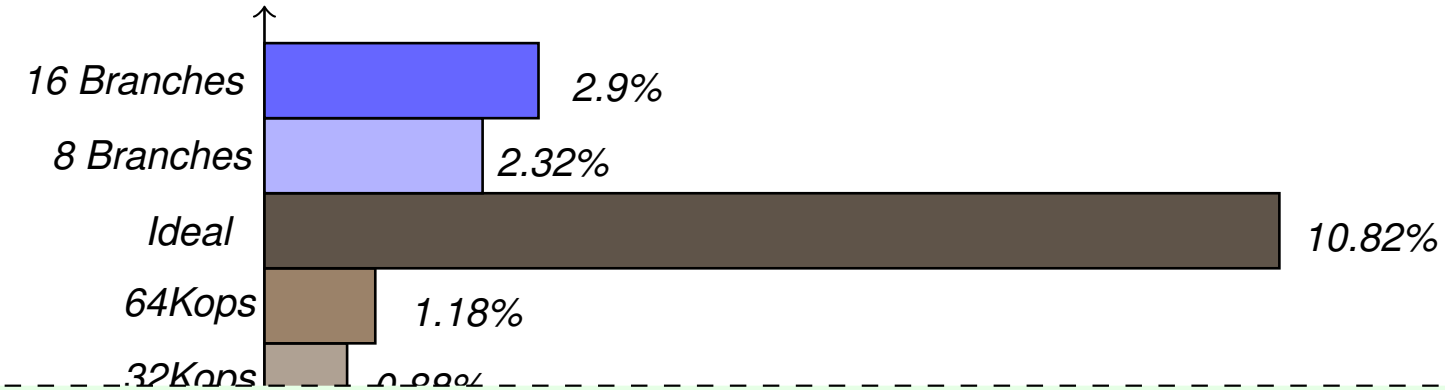

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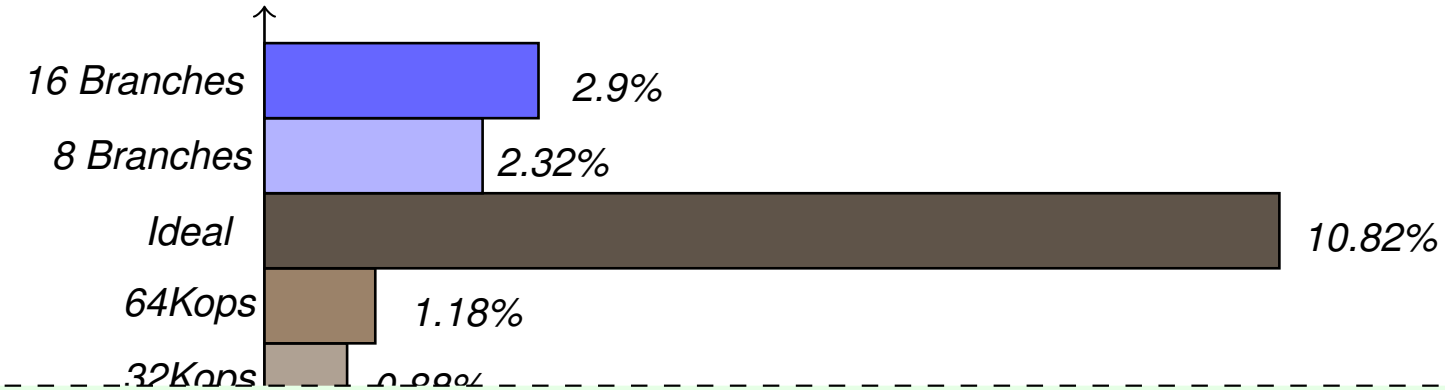

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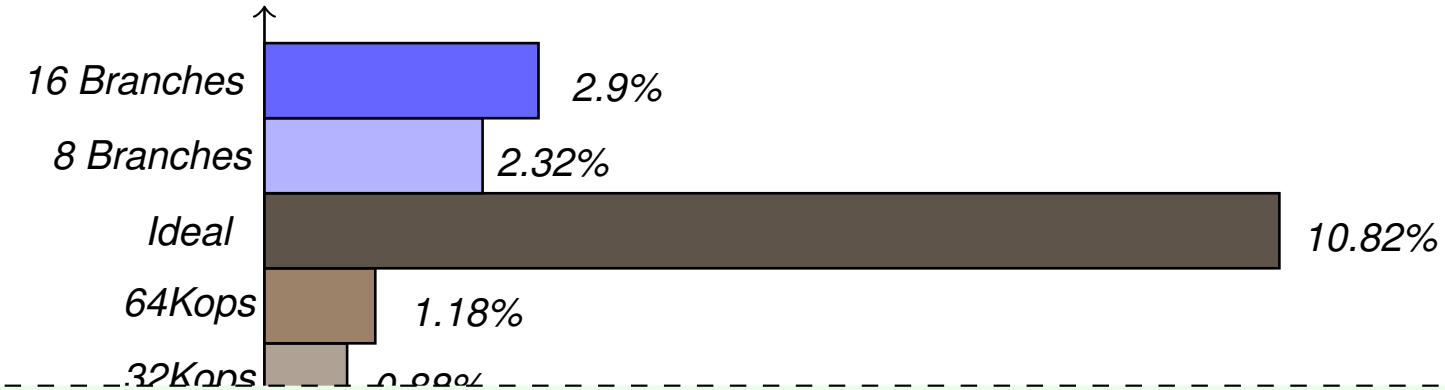

Key Insight:

1. *FTQ is unable to hide the fetch latency on branch misprediction*

2. *Focusing on few but critical instructions can provide significant performance benefits*

Outline

1. Overview
2. Background & Motivation
3. UCP
4. Methodology & Results
5. Conclusions

UCP: Overview

① Identifies a hard-to-predict conditional branch (H2P)

UCP

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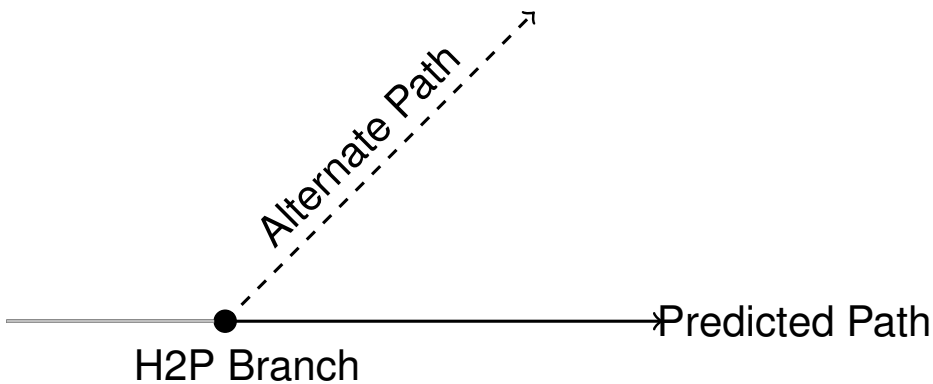

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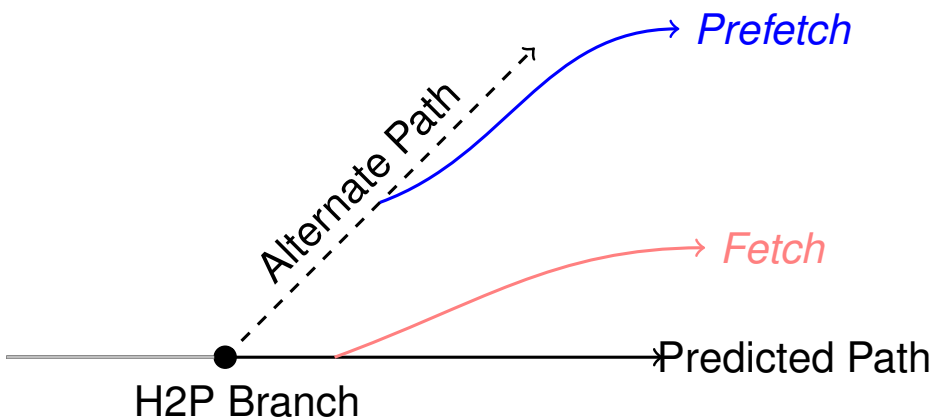

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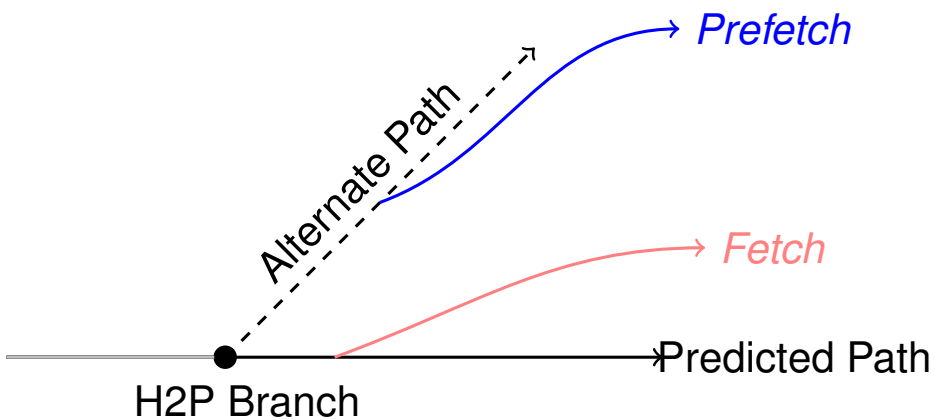

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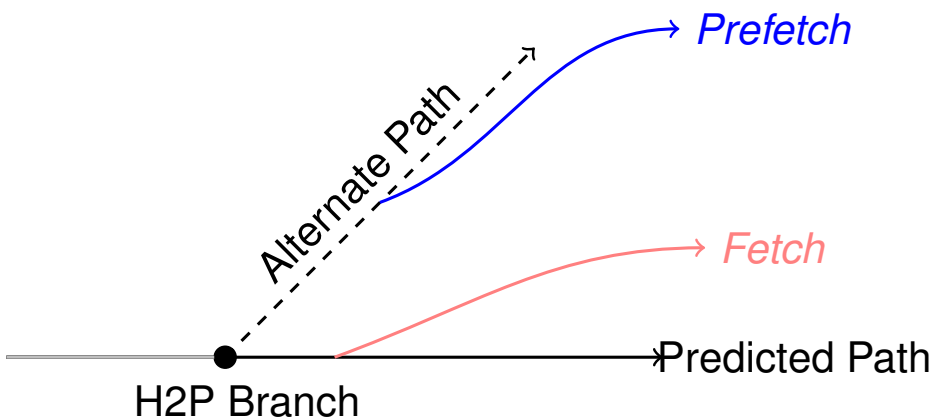

Key Idea: *Keep the alternate path in the μ-op cache for H2P branches*

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→ H2P Branch: a branch which has high chance of being mispredicted

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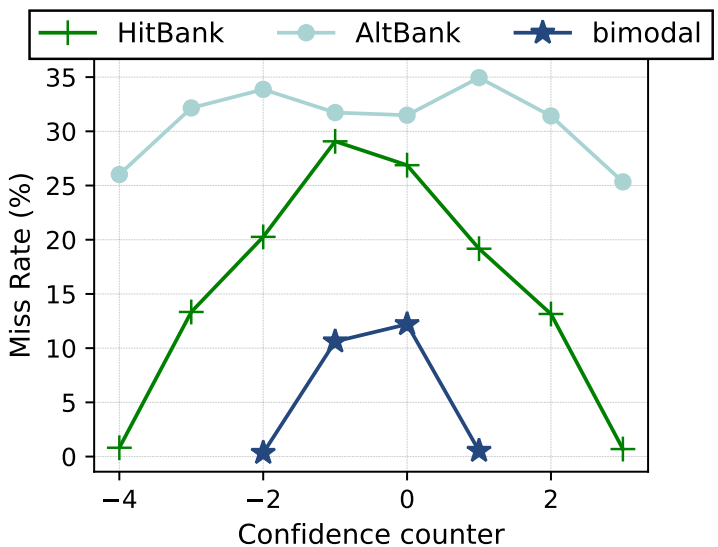

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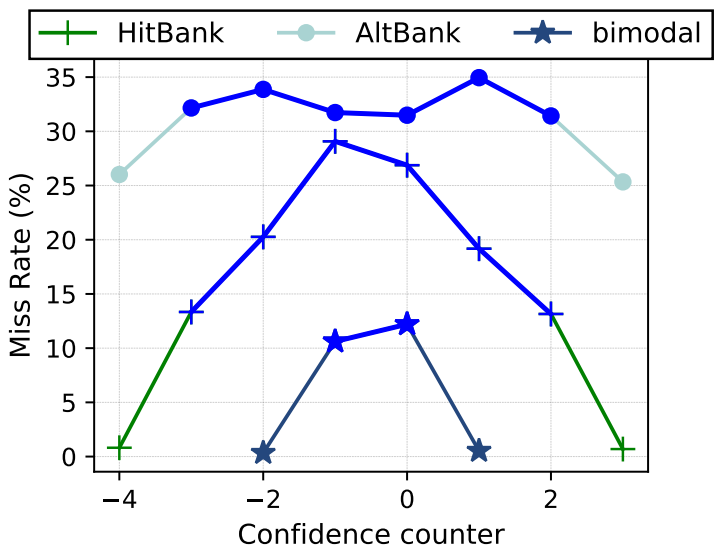

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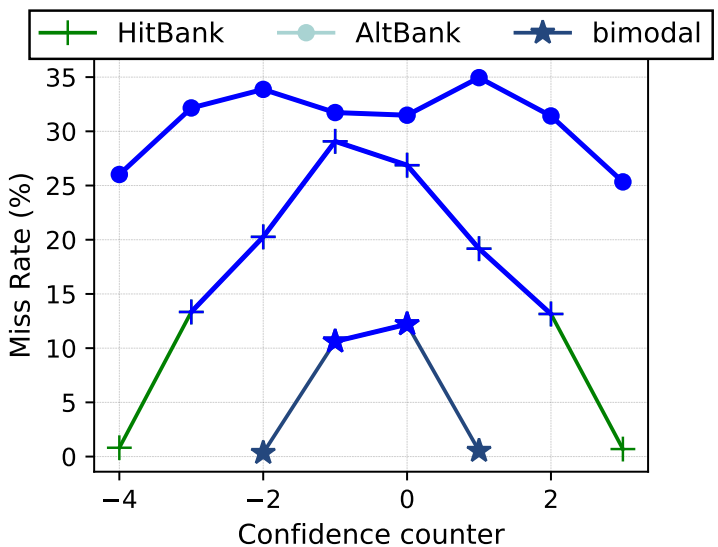

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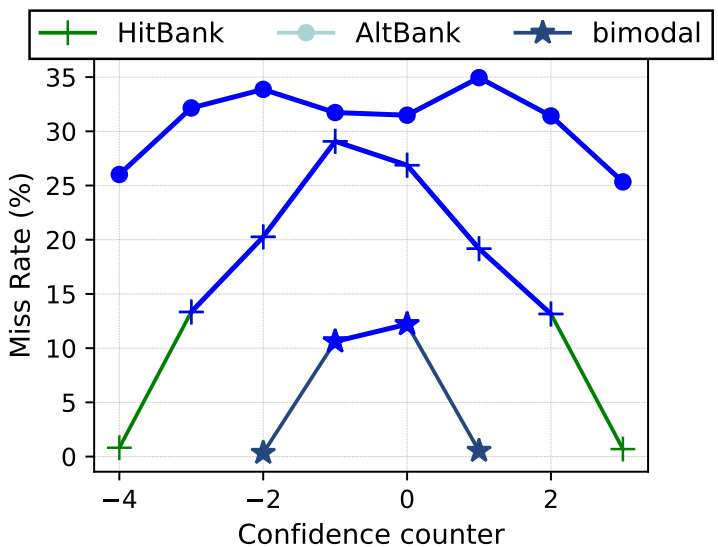

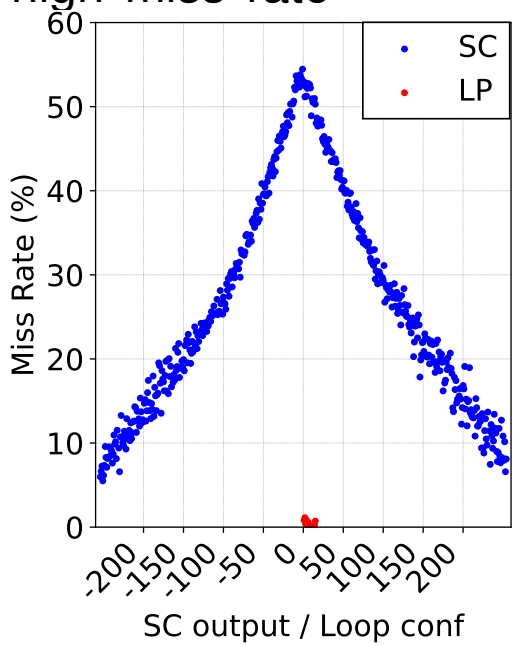

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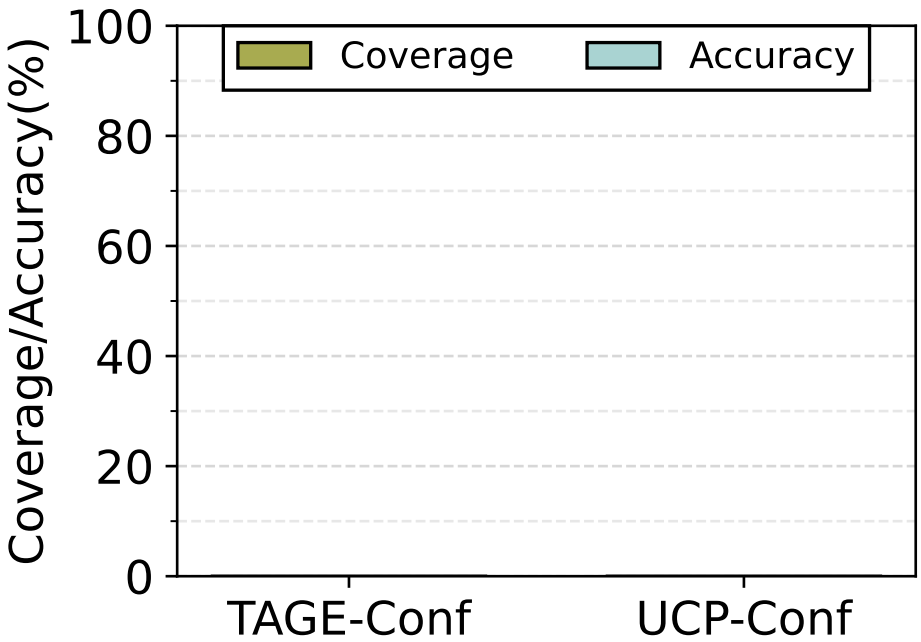

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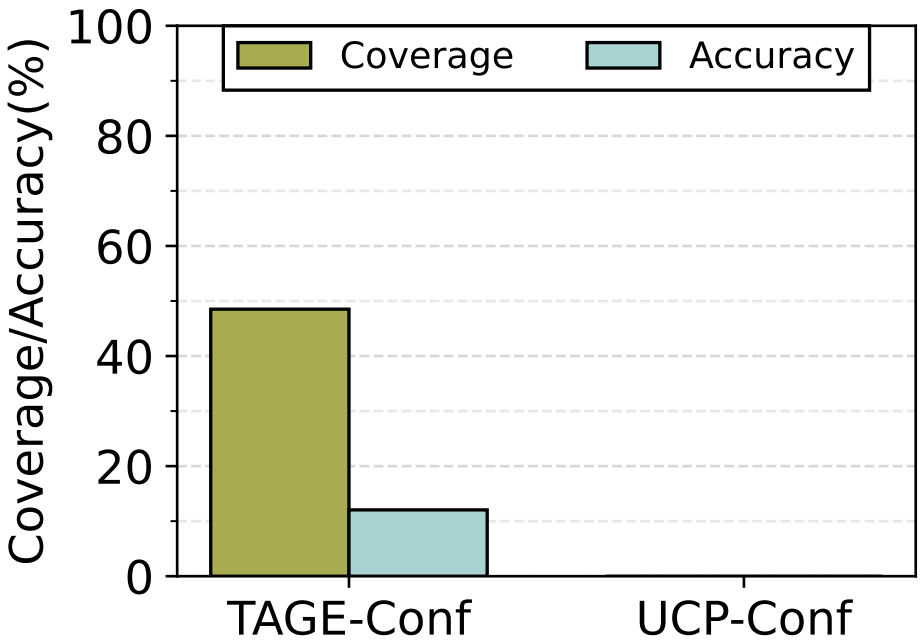

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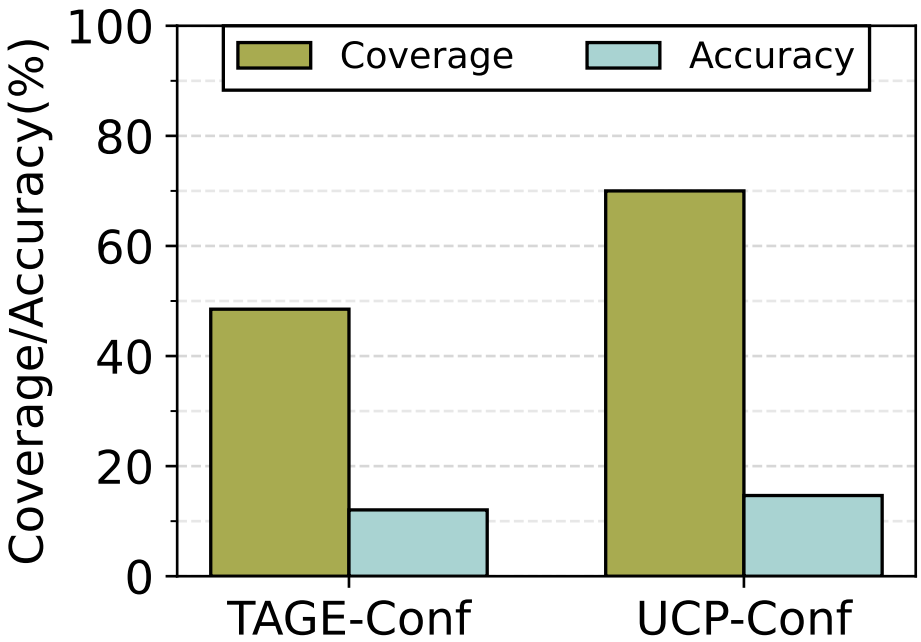


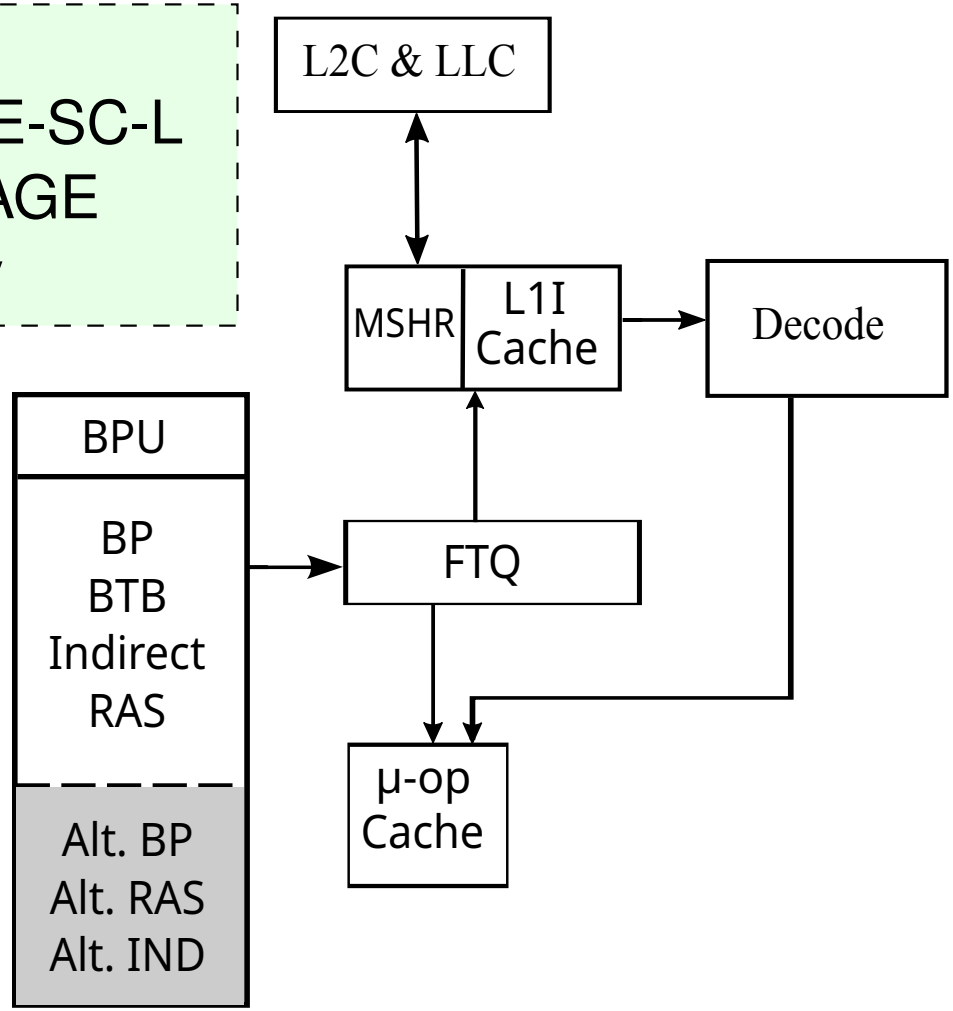
→ TAGE-Conf provide 48.5% coverage and 12% accuracy

→ UCP-Conf improve coverage to 70% and accuracy to 14.66%

UCP

UCP: Design

BTB: Shared
Alt BP: 8KB TAGE-SC-L
Alt IND: 4KB ITTAGE
Alt RAS: 16-entry



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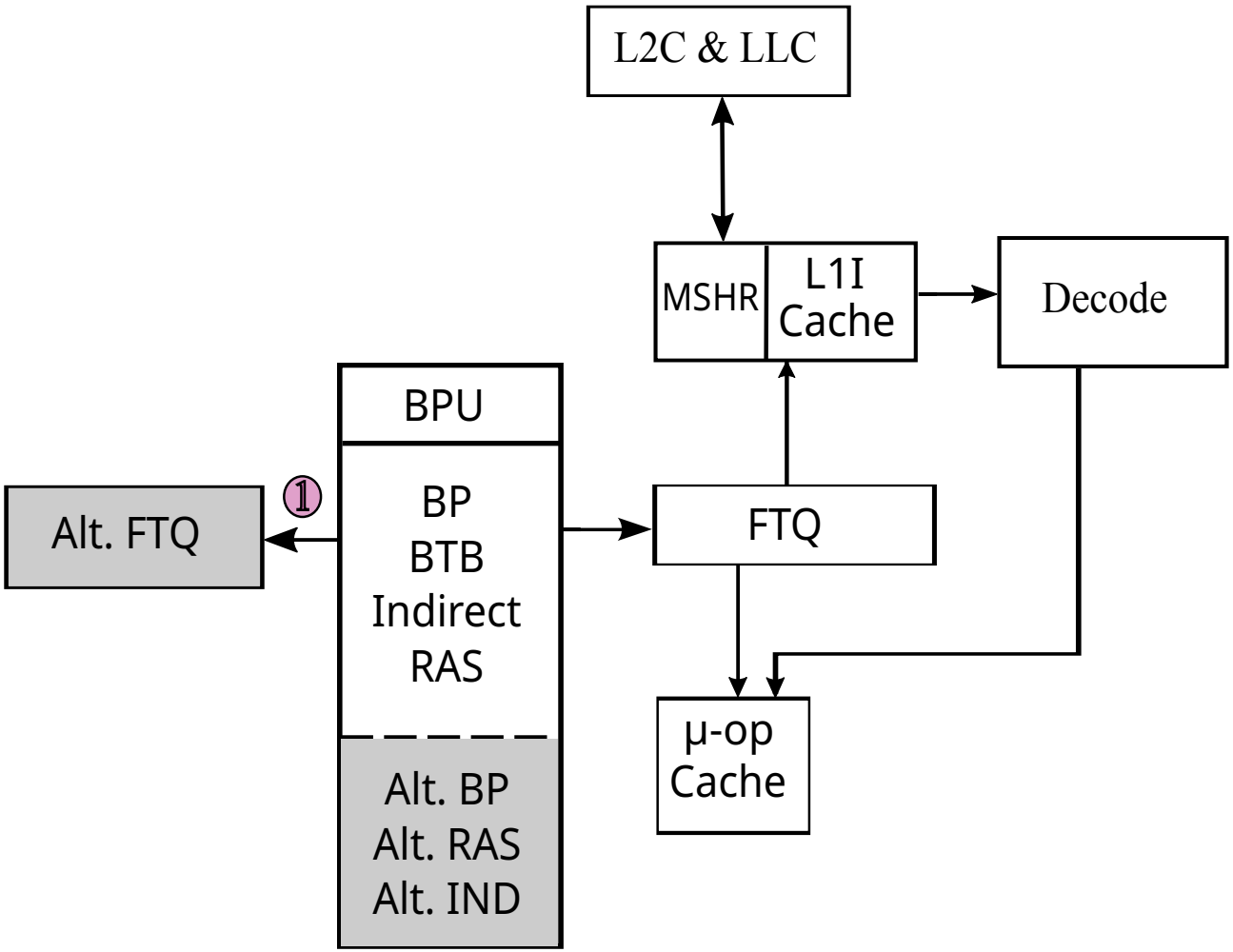

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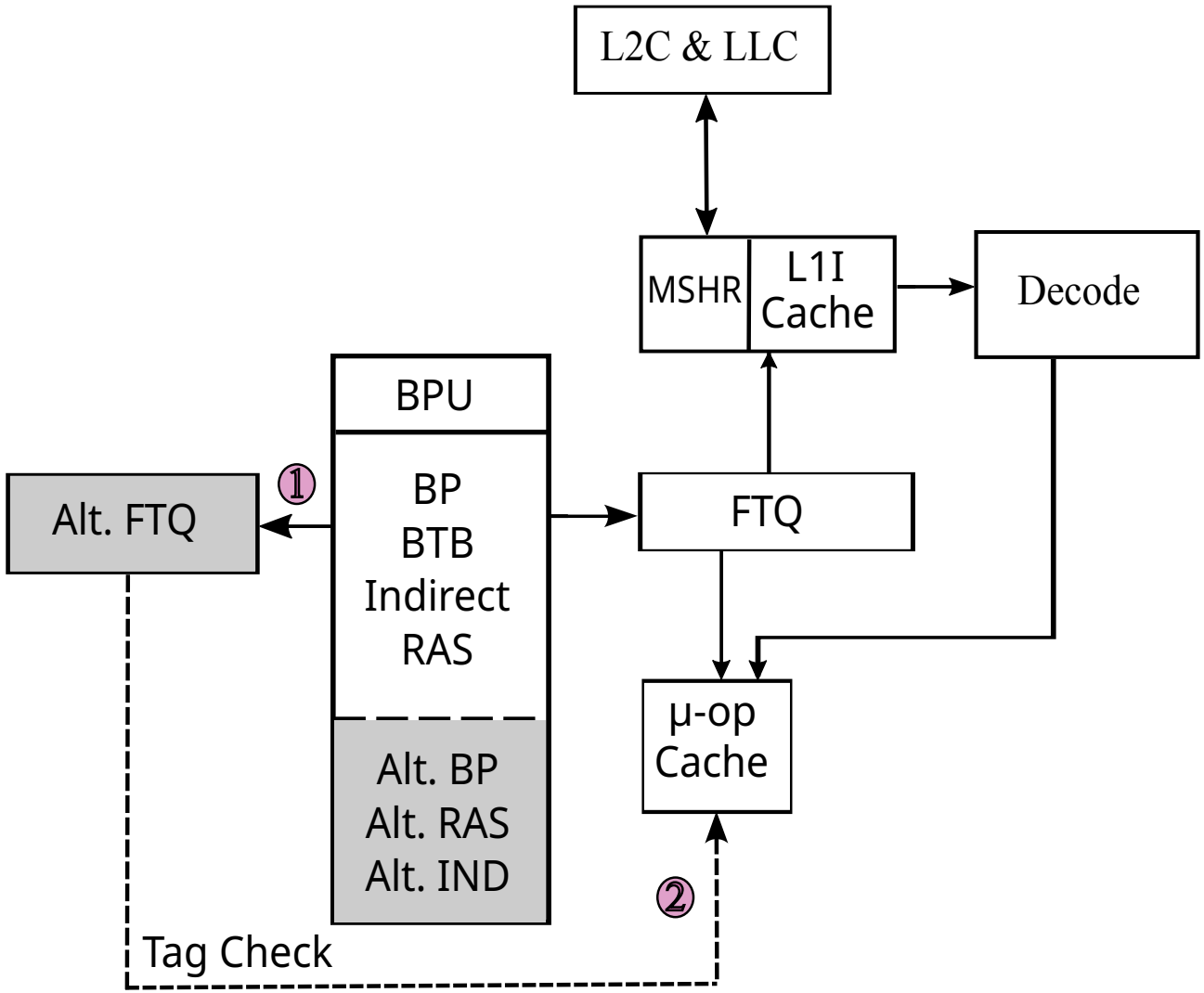

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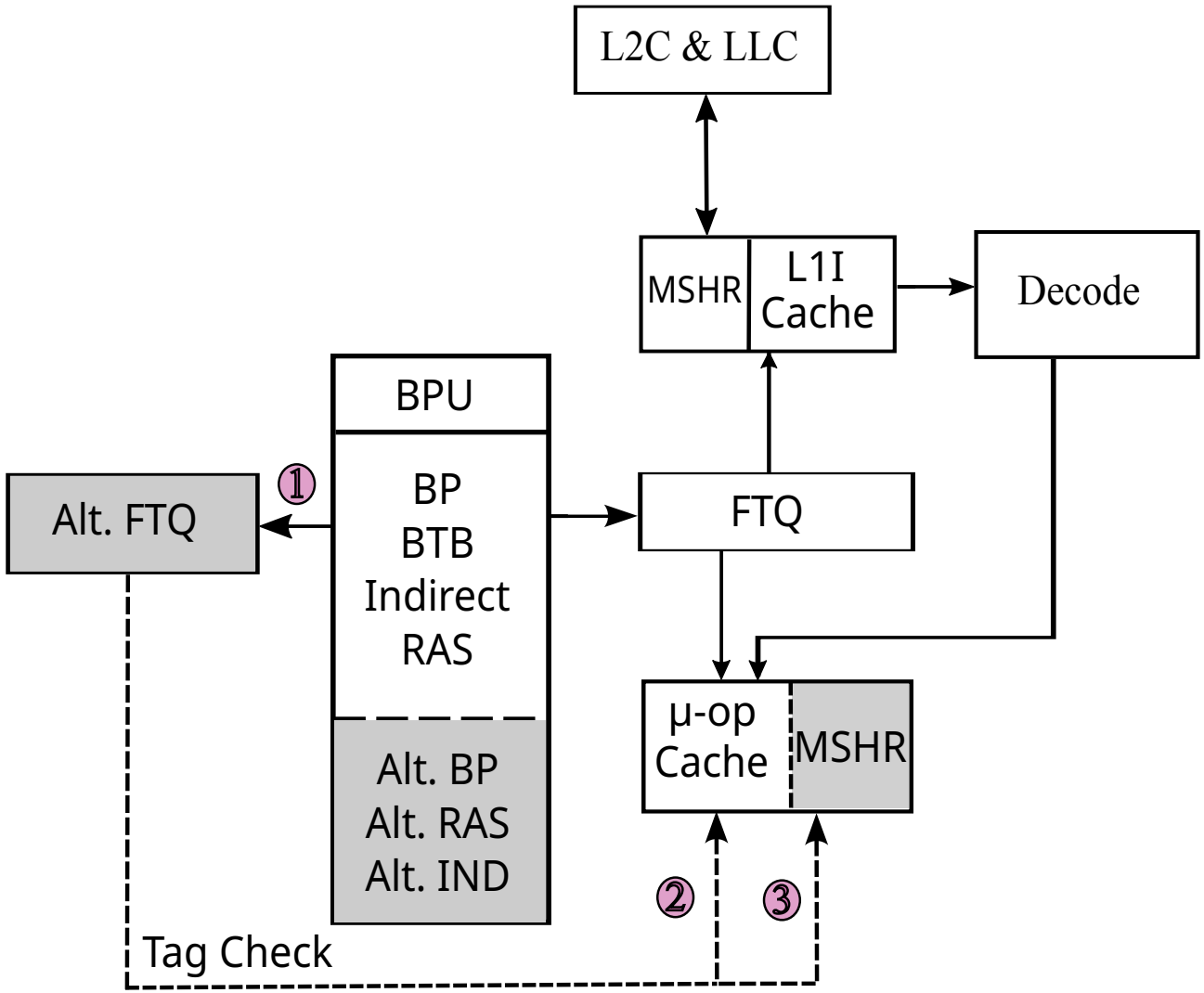

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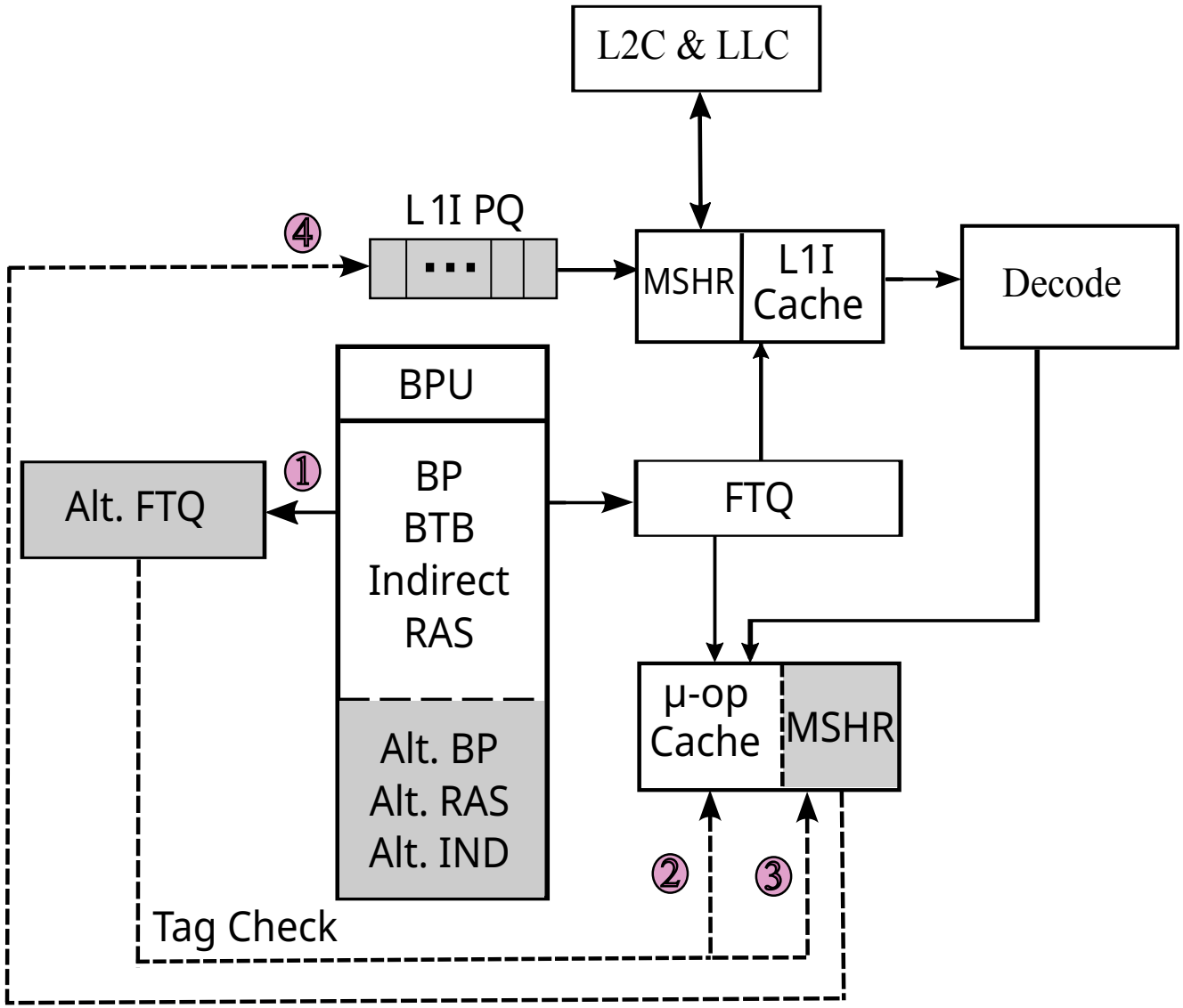

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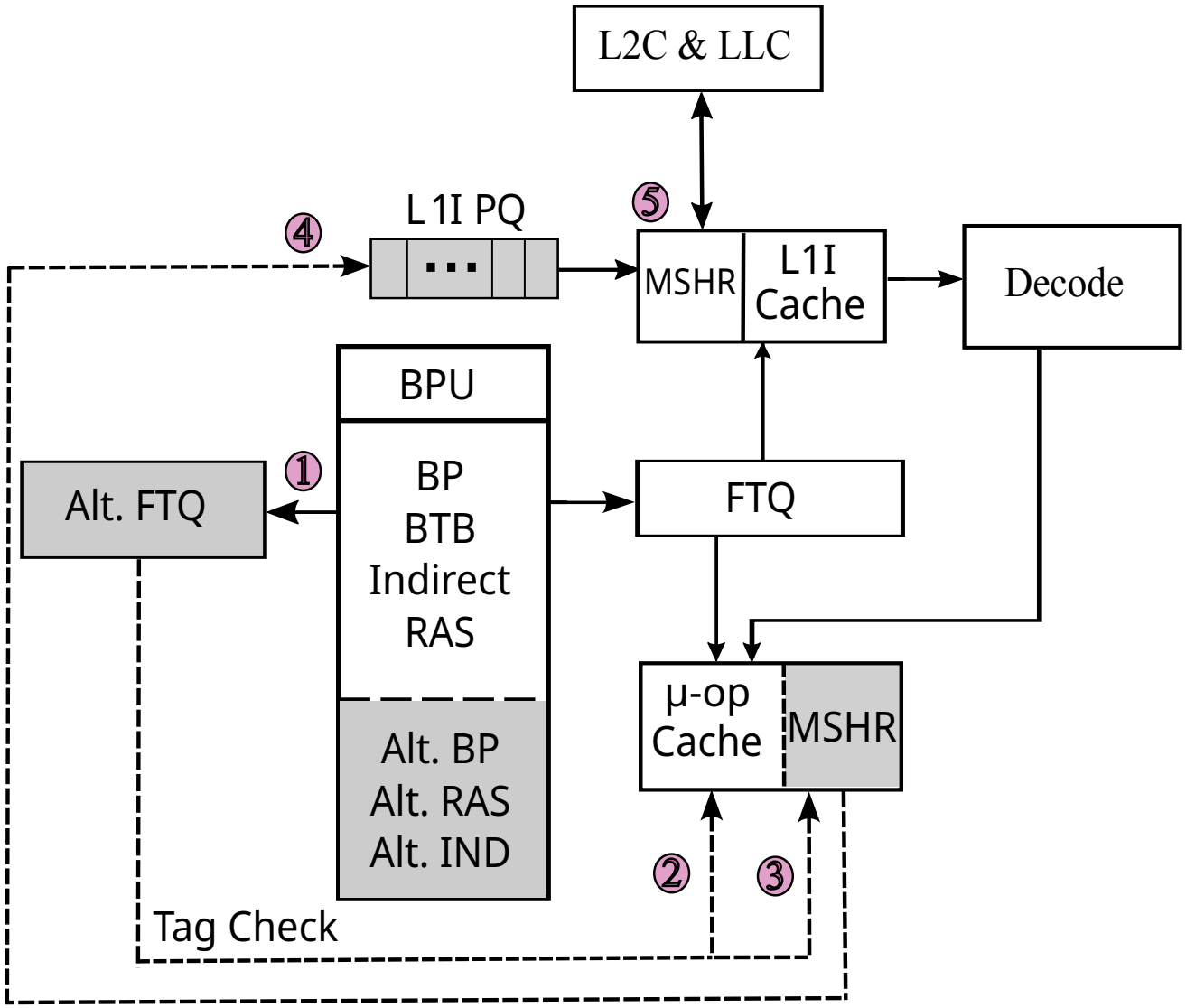

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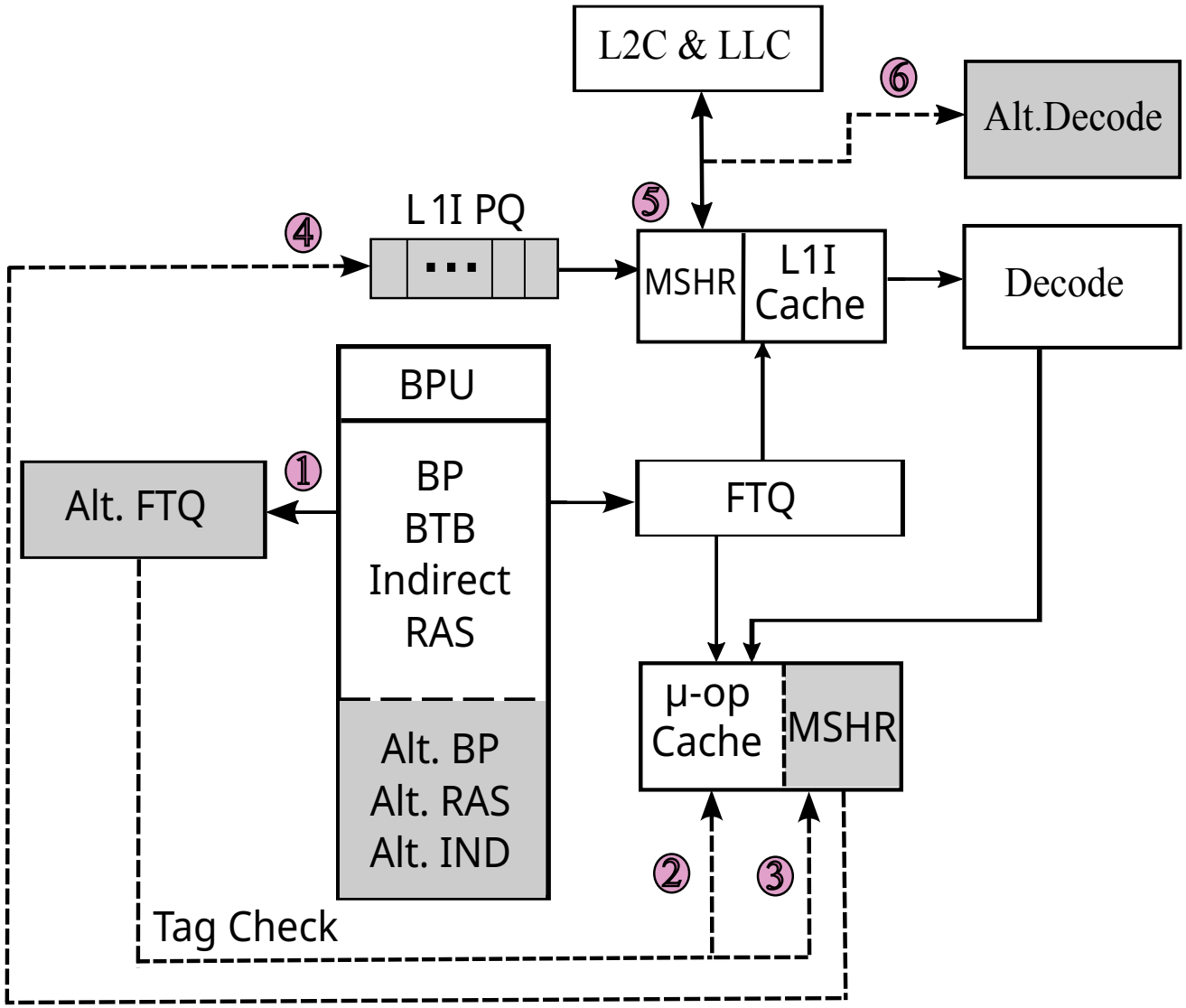

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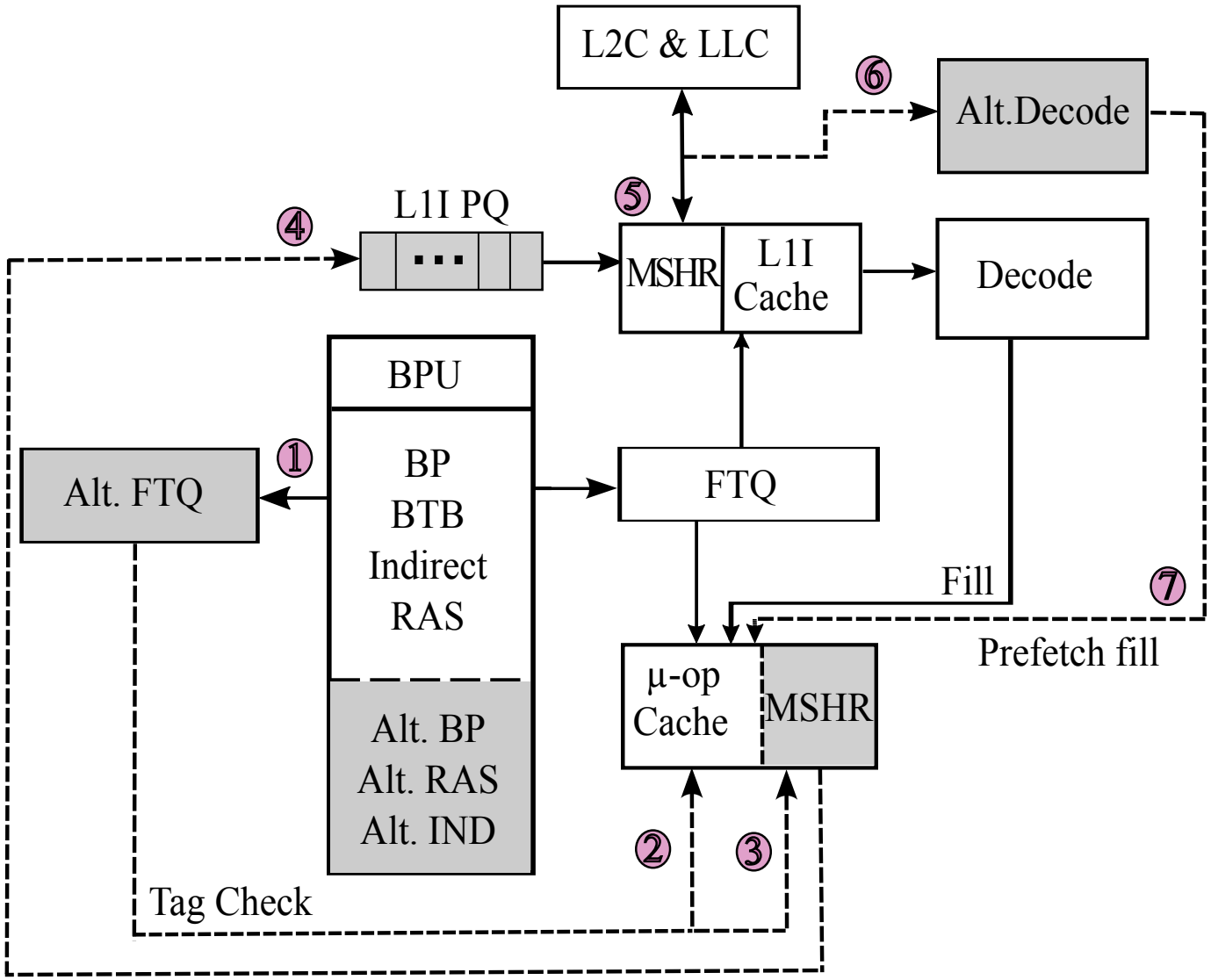

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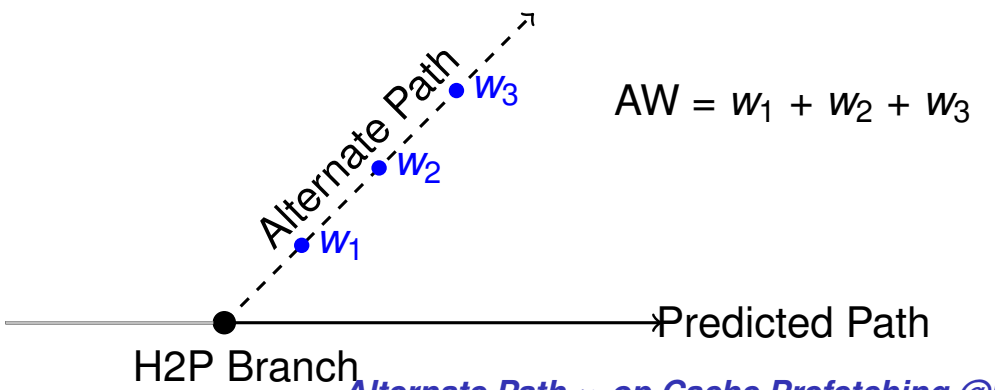

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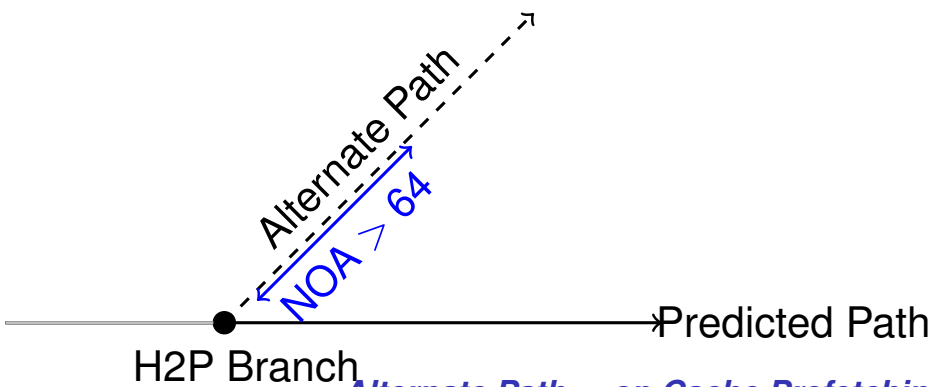

Outline

1. Overview
2. Background & Motivation
3. UCP
4. Methodology & Results
5. Conclusions

METHODOLOGY & RESULTS

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→ ChampSim + subset (traces showing $\geqq$ 5% improvement with ideal μ-op cache) of CVP traces (2 FP, 97 INT, 73 Crypto and 134 datacenter trace)

Methodology & Results

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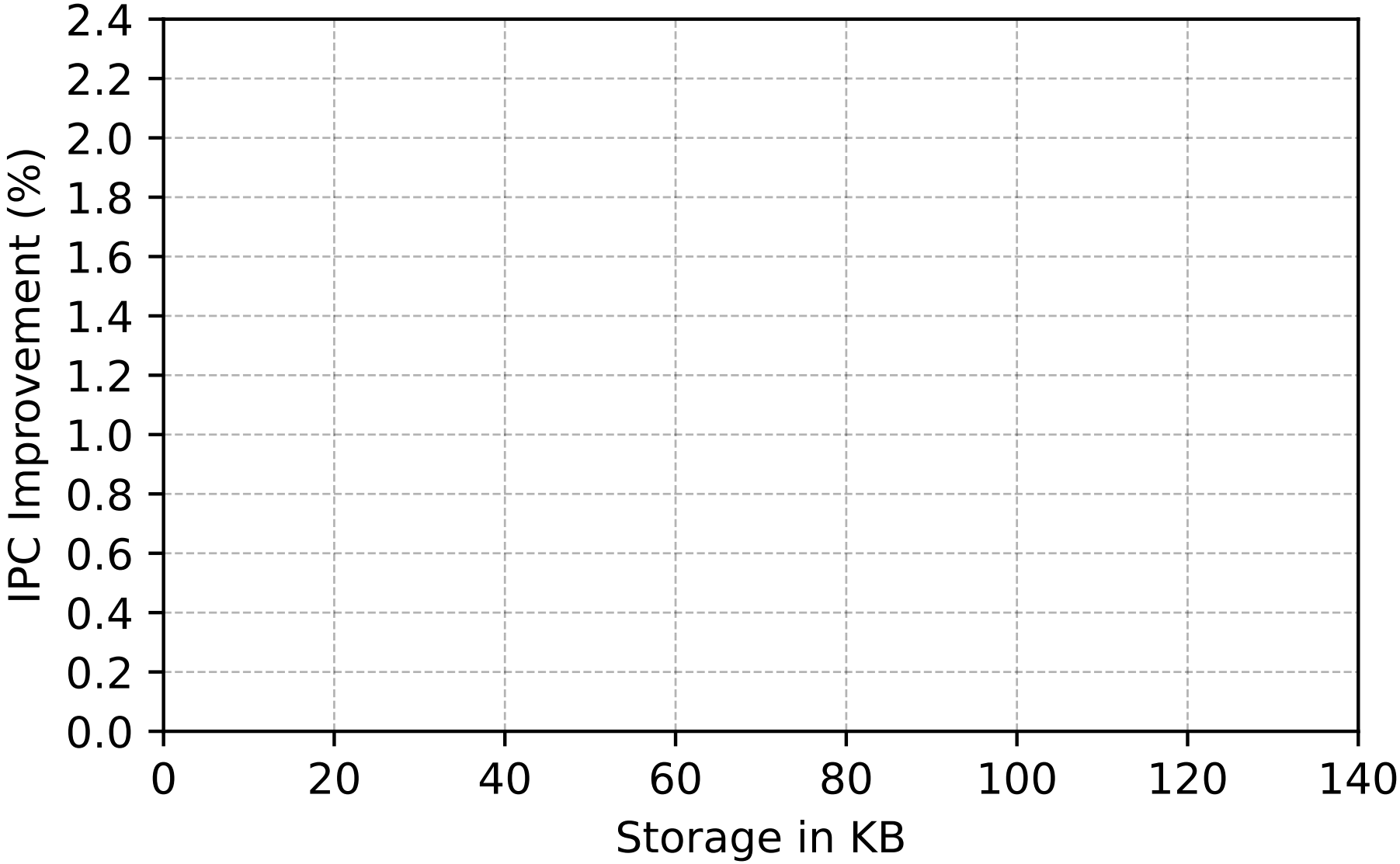
- → 1 cycle penalty for switching from μ-op cache to L1I cache

METHODOLOGY & RESULTS

IPC IMPROVEMENTS



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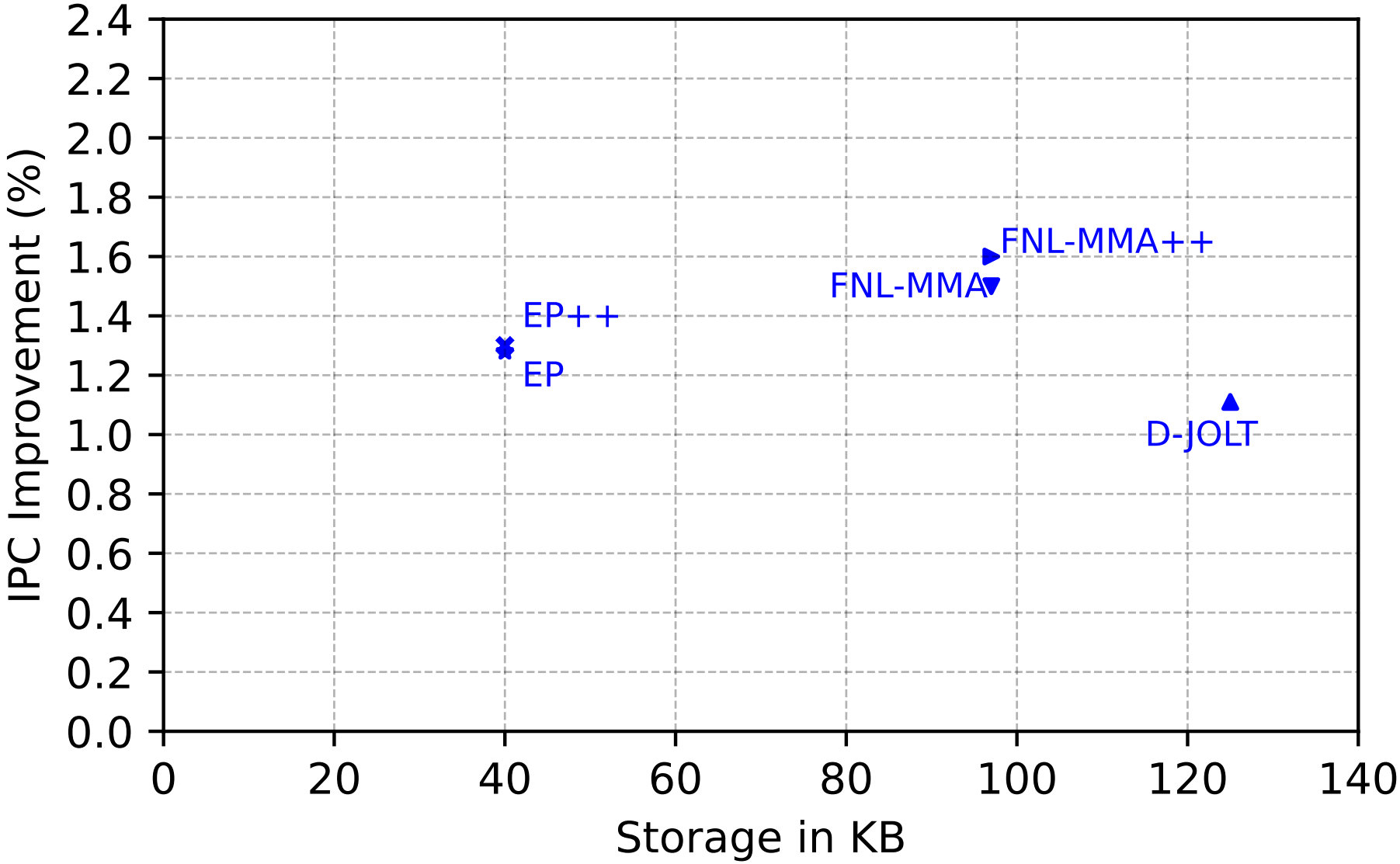

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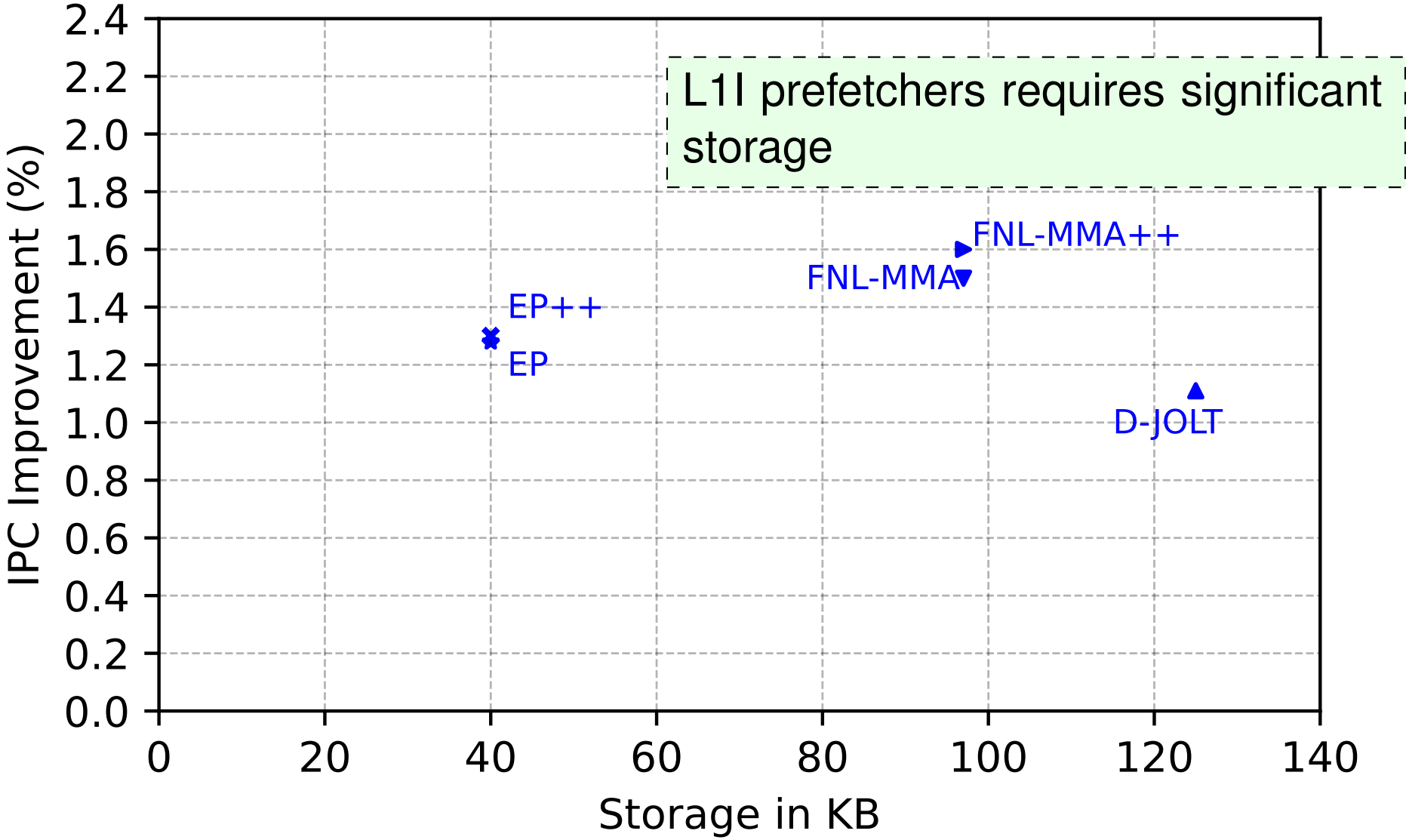

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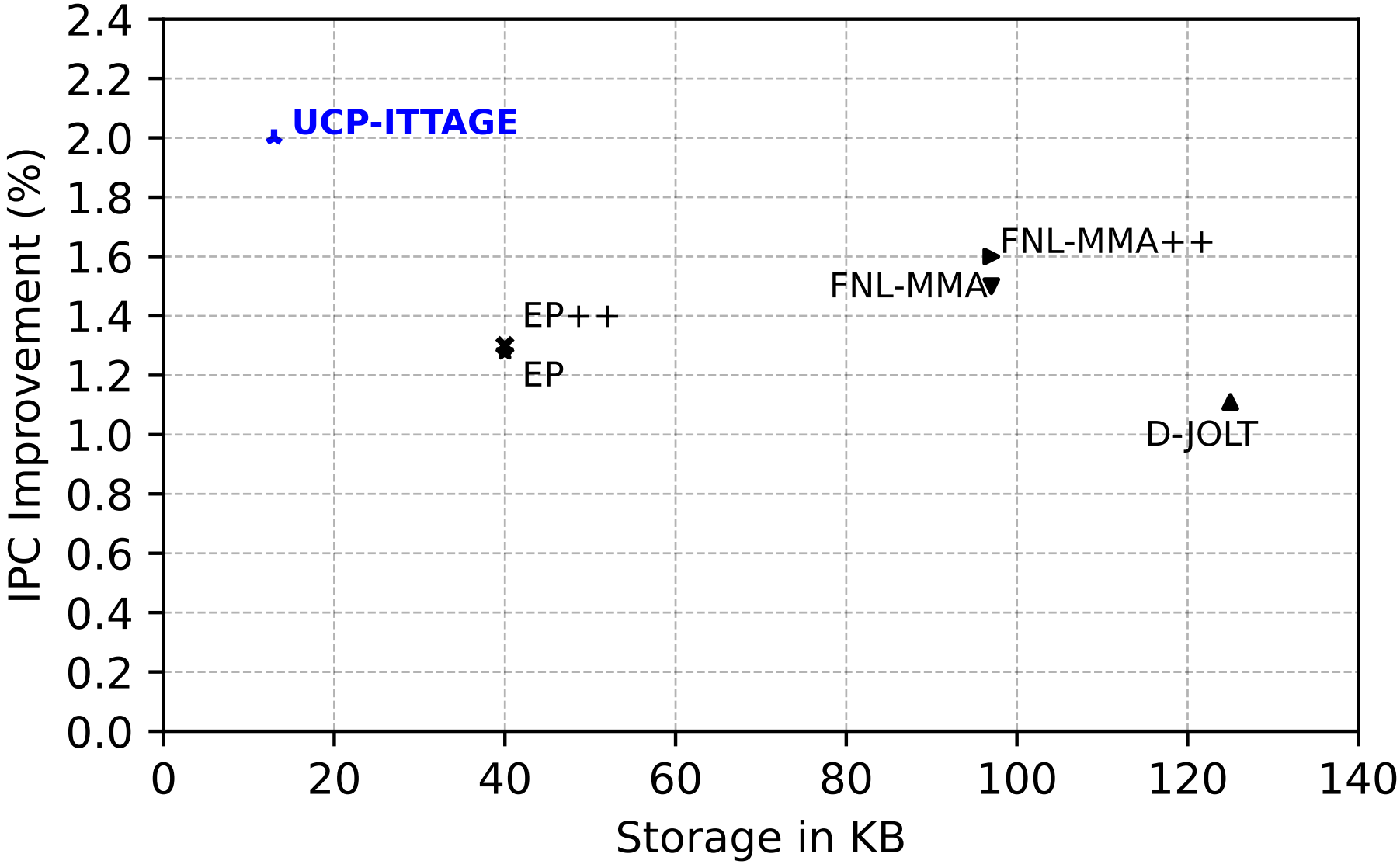

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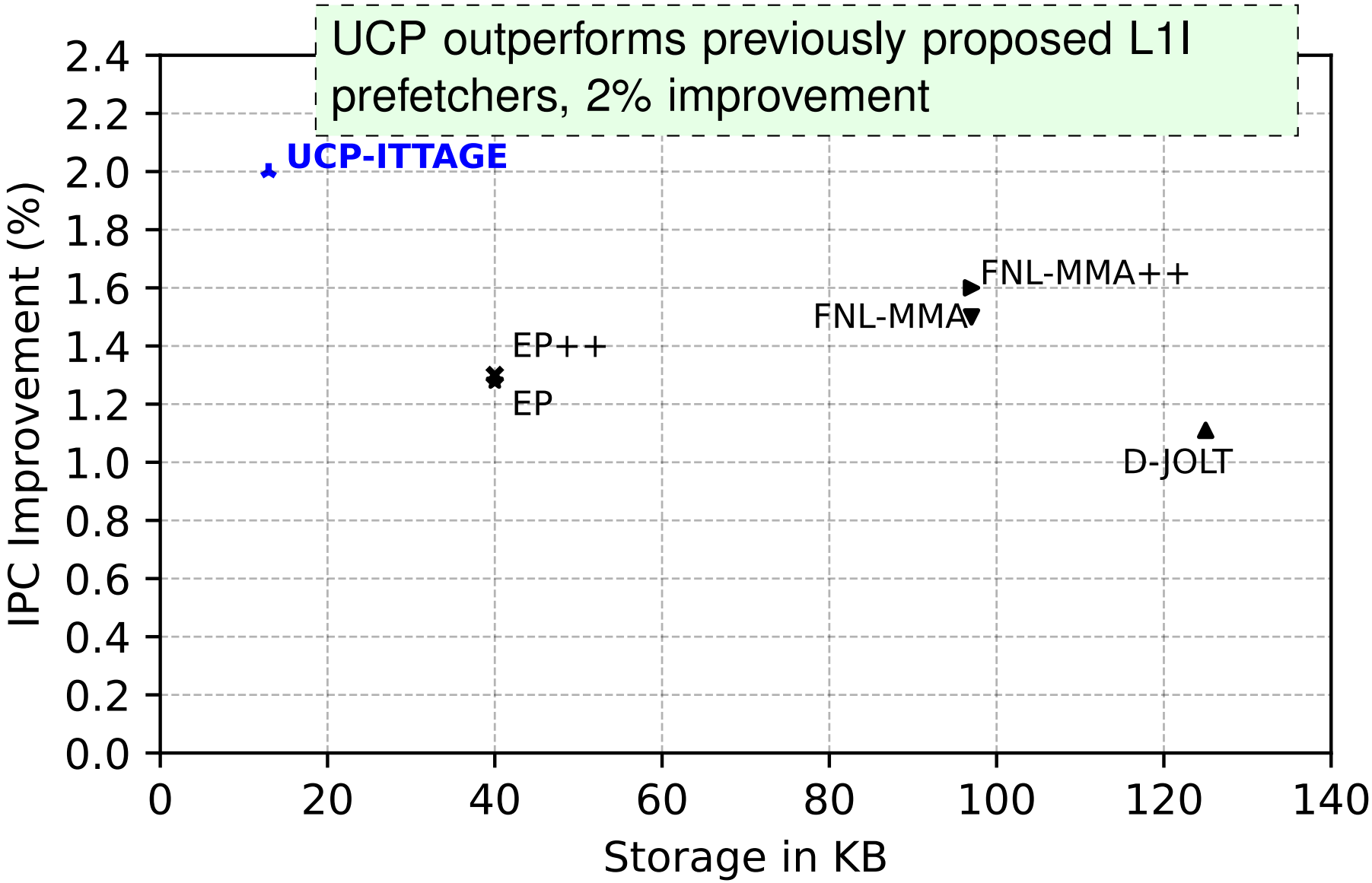

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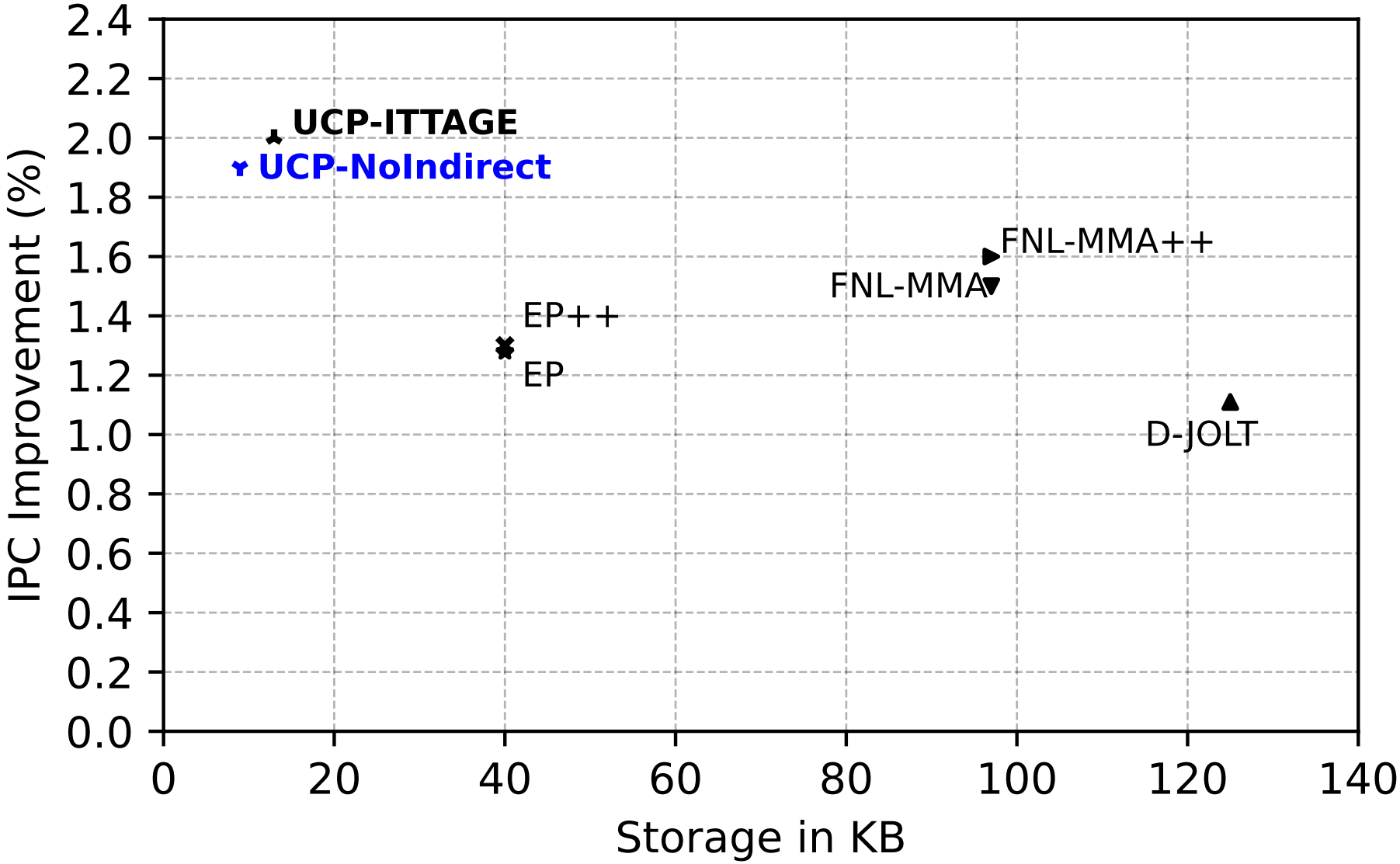

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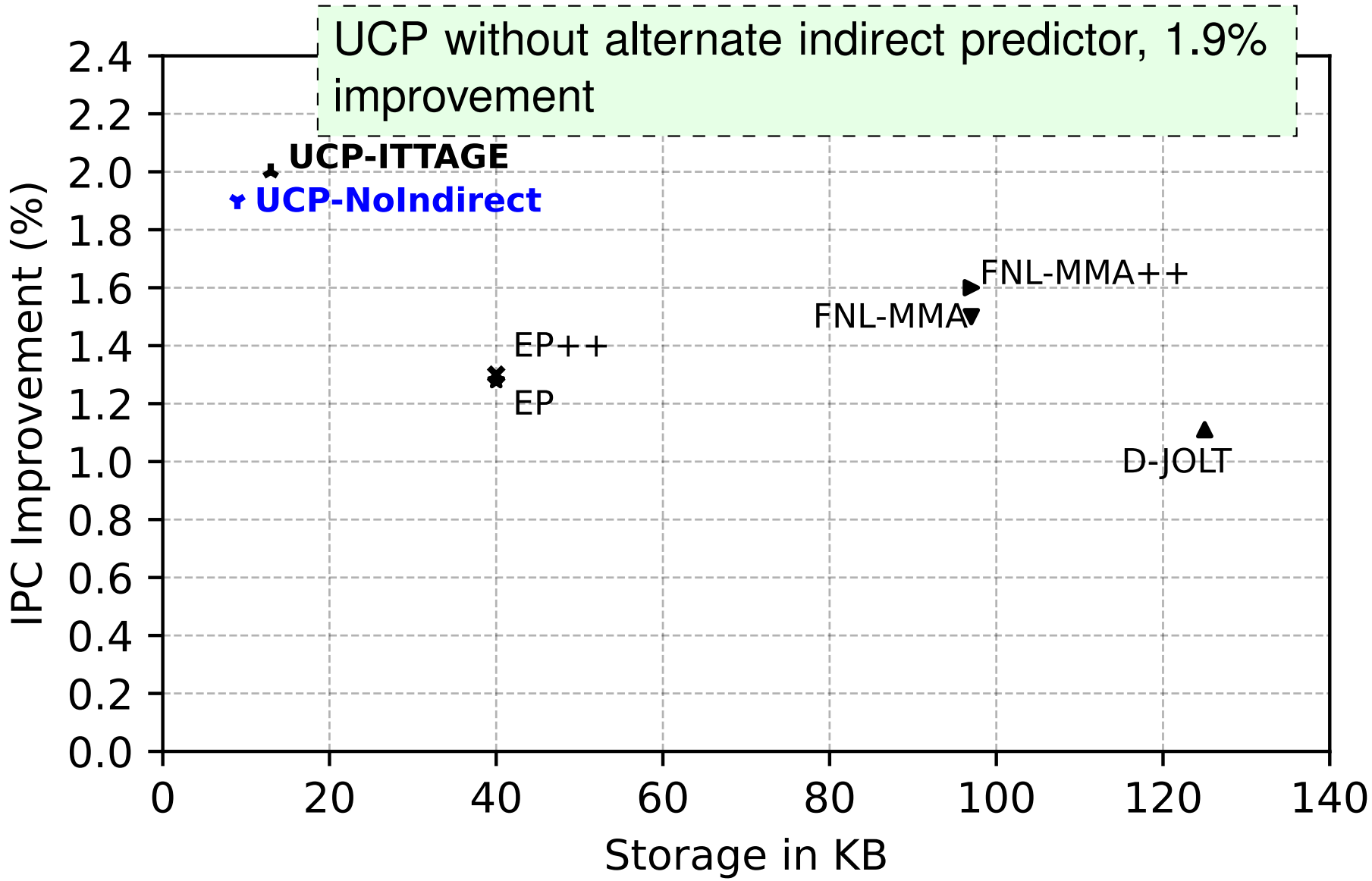

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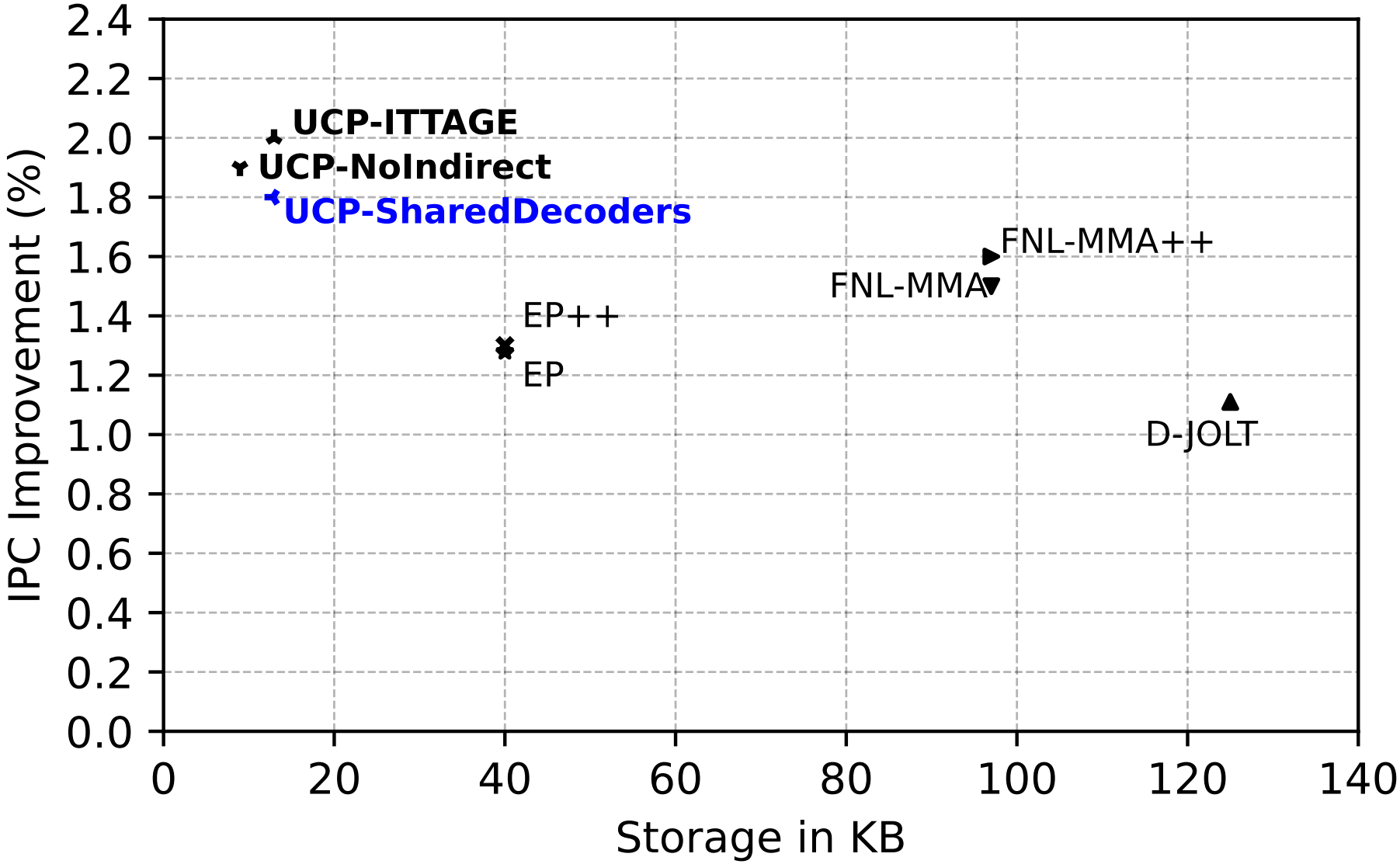

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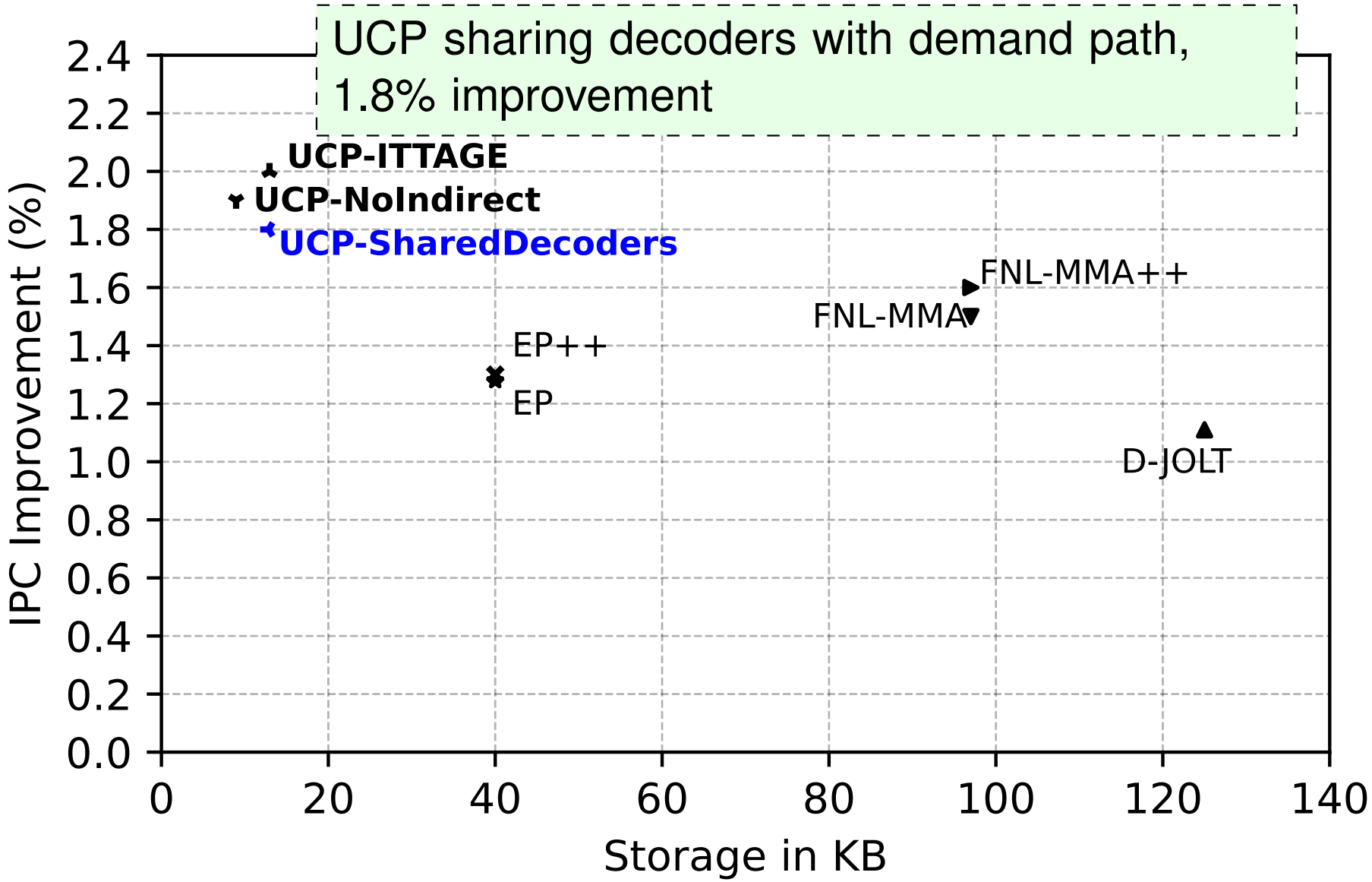

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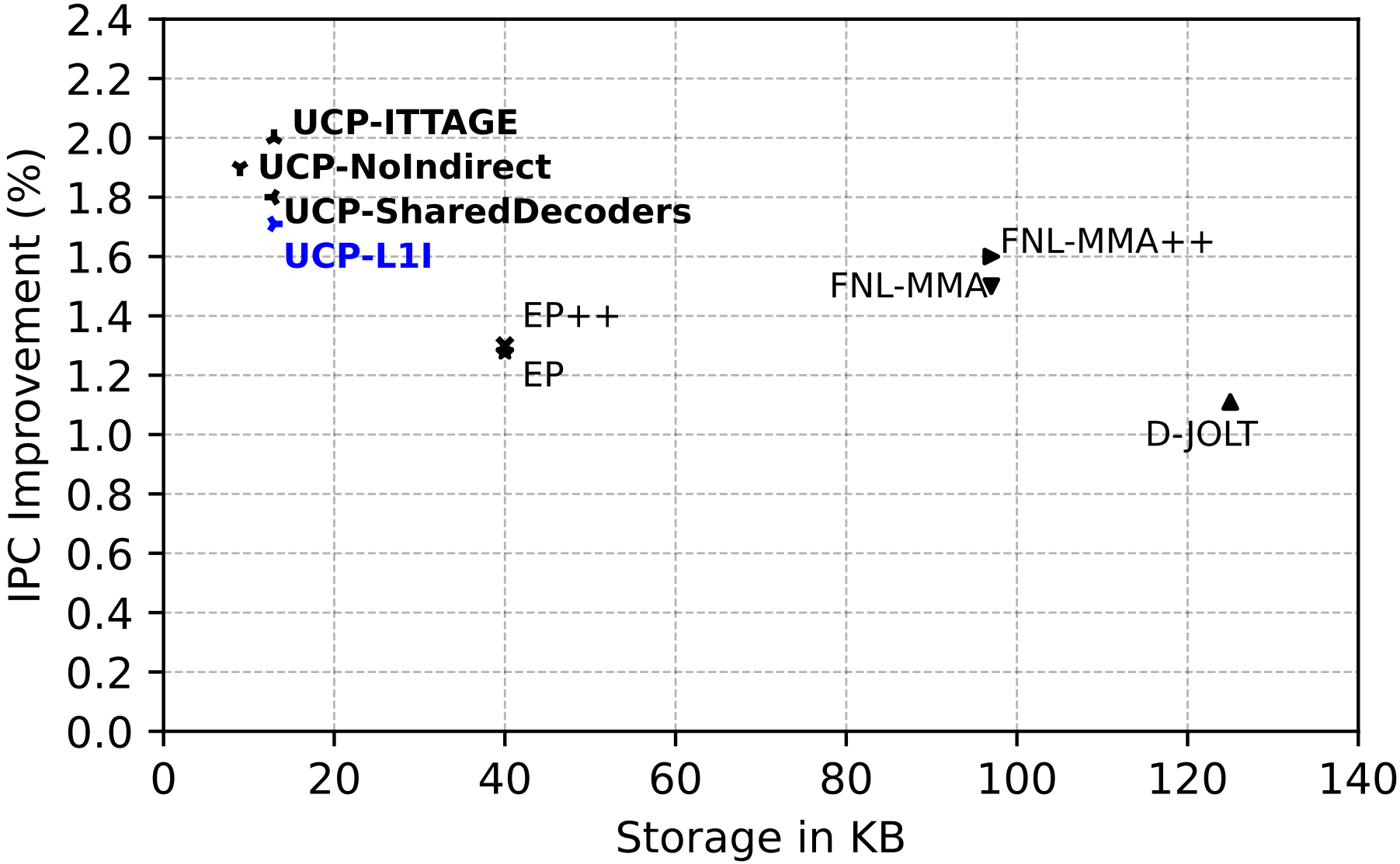

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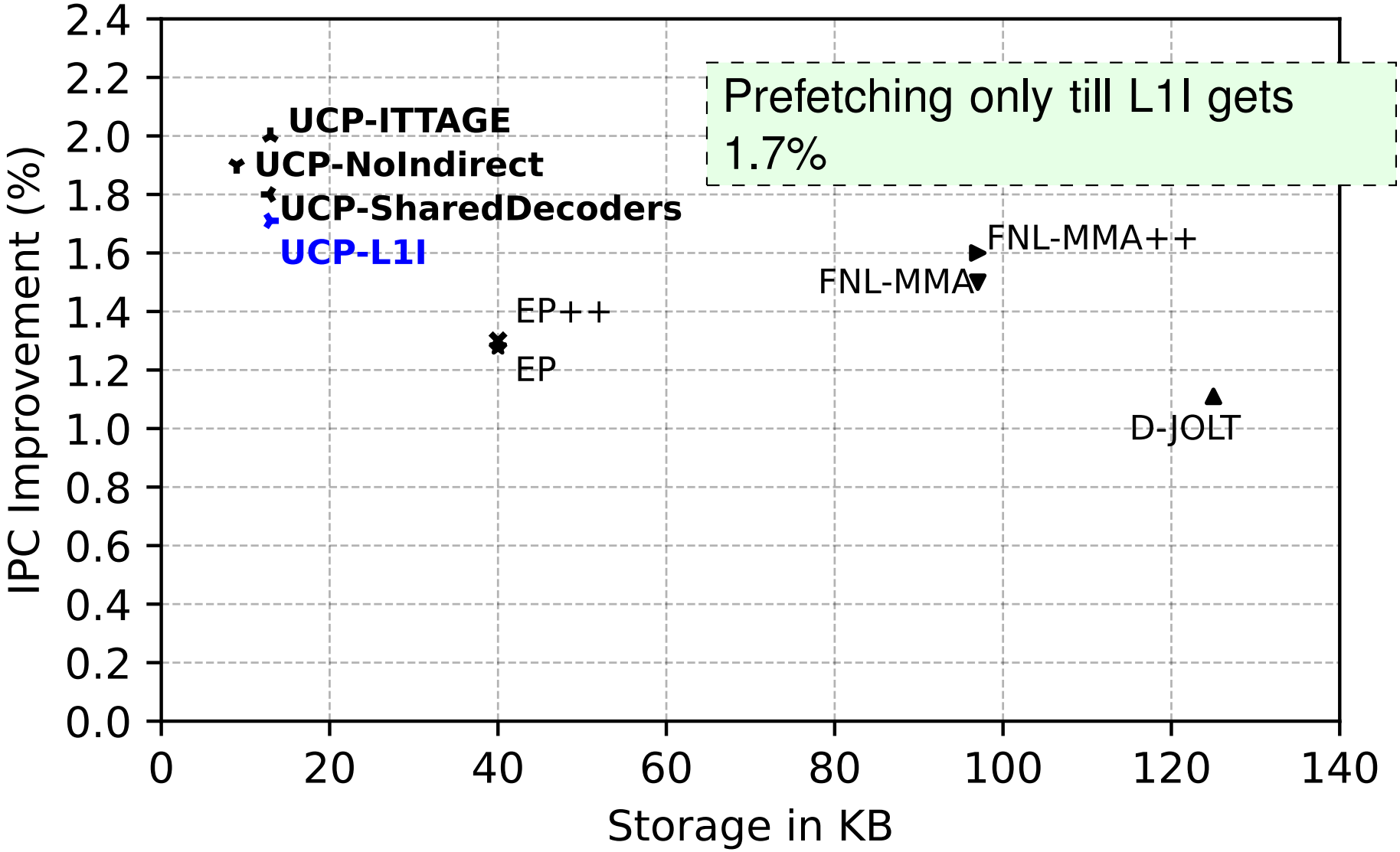

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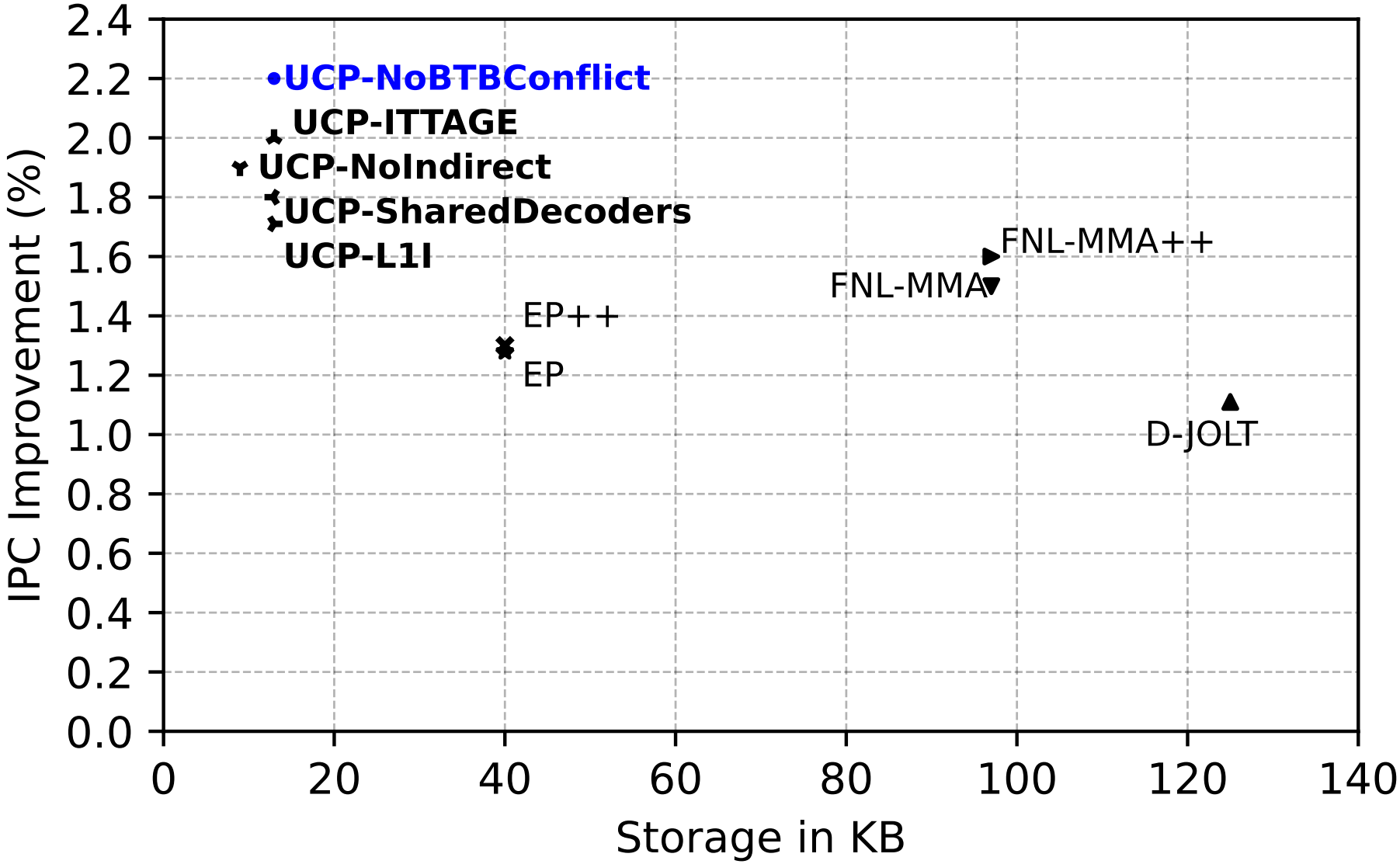

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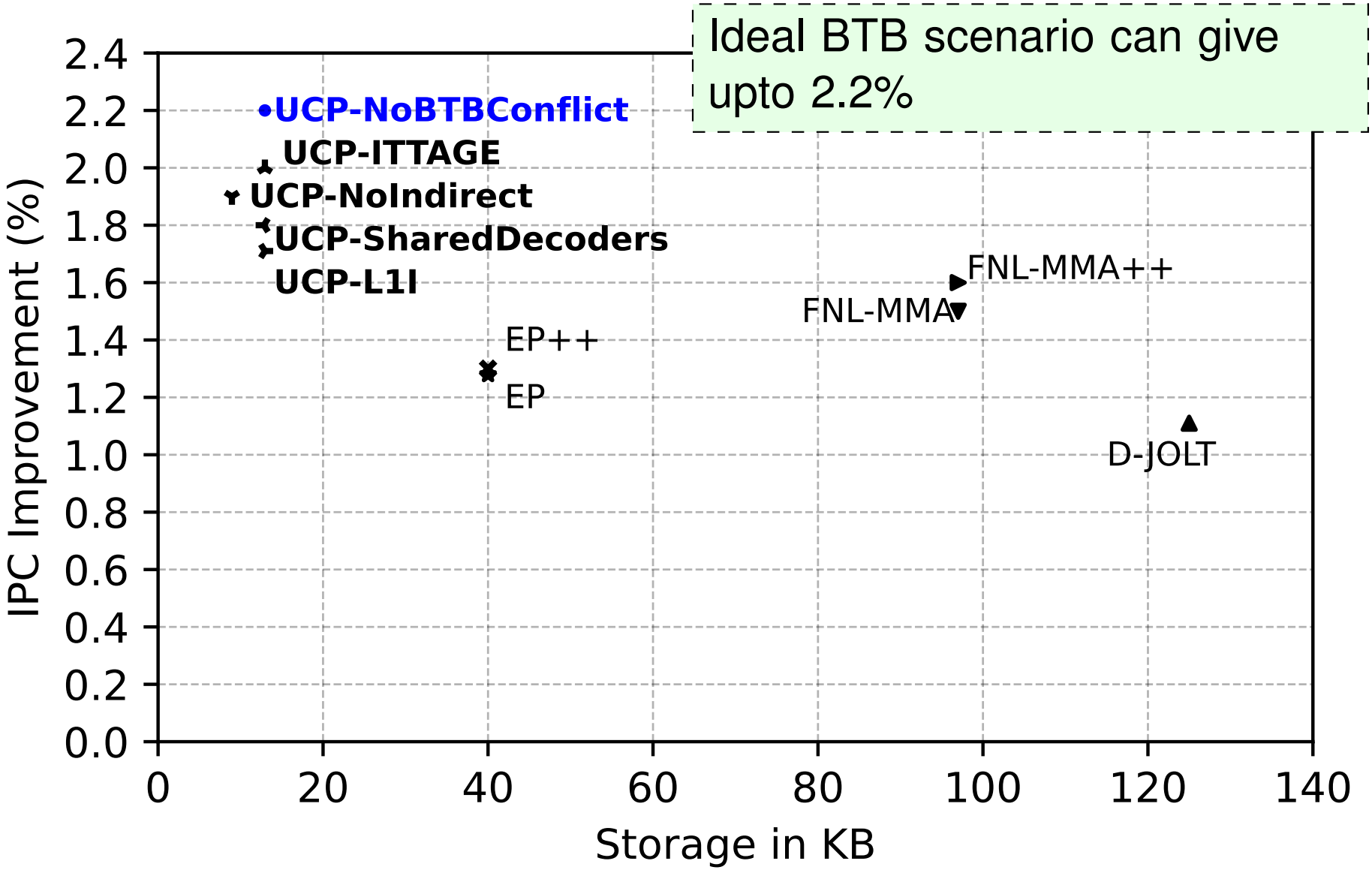

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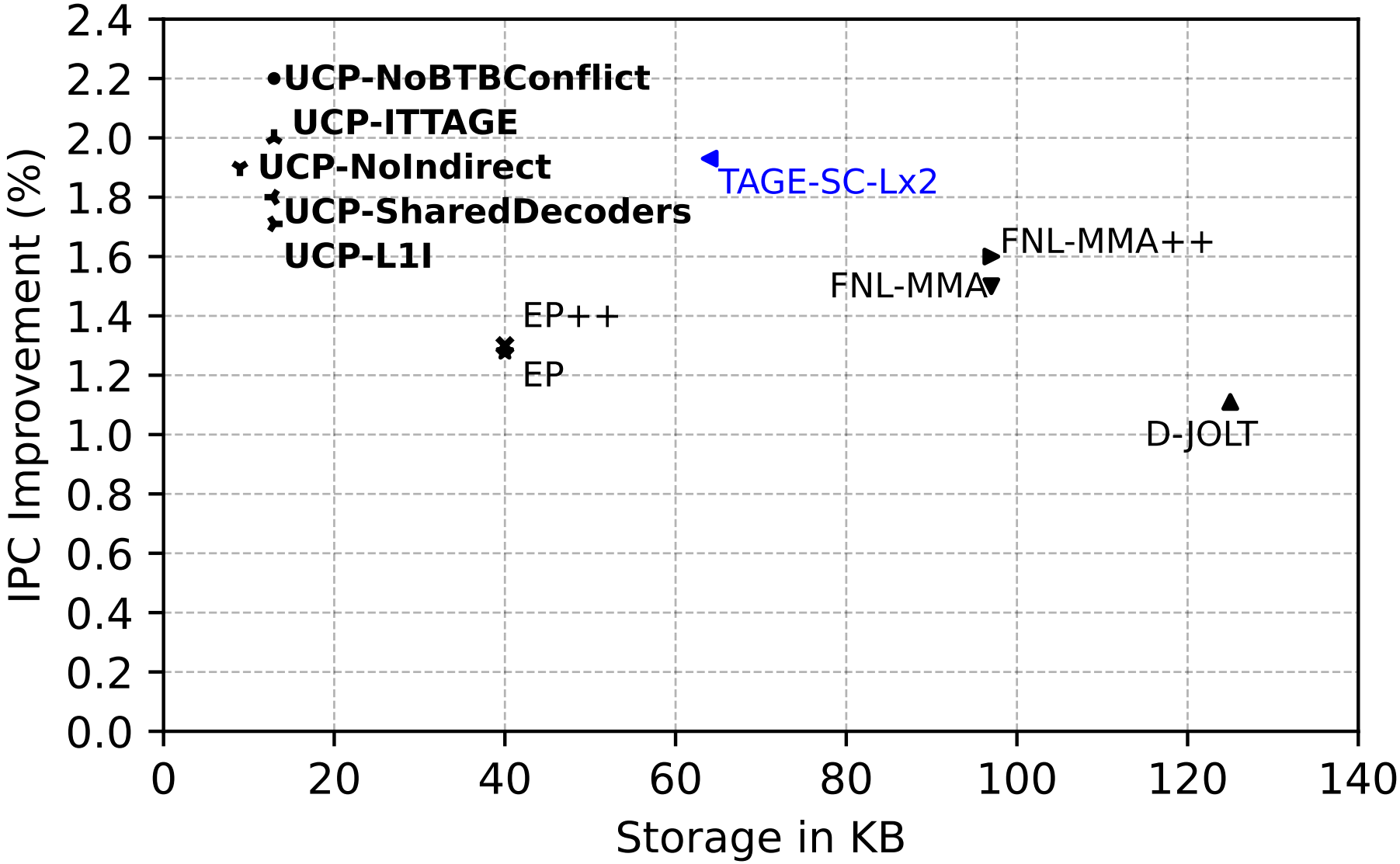

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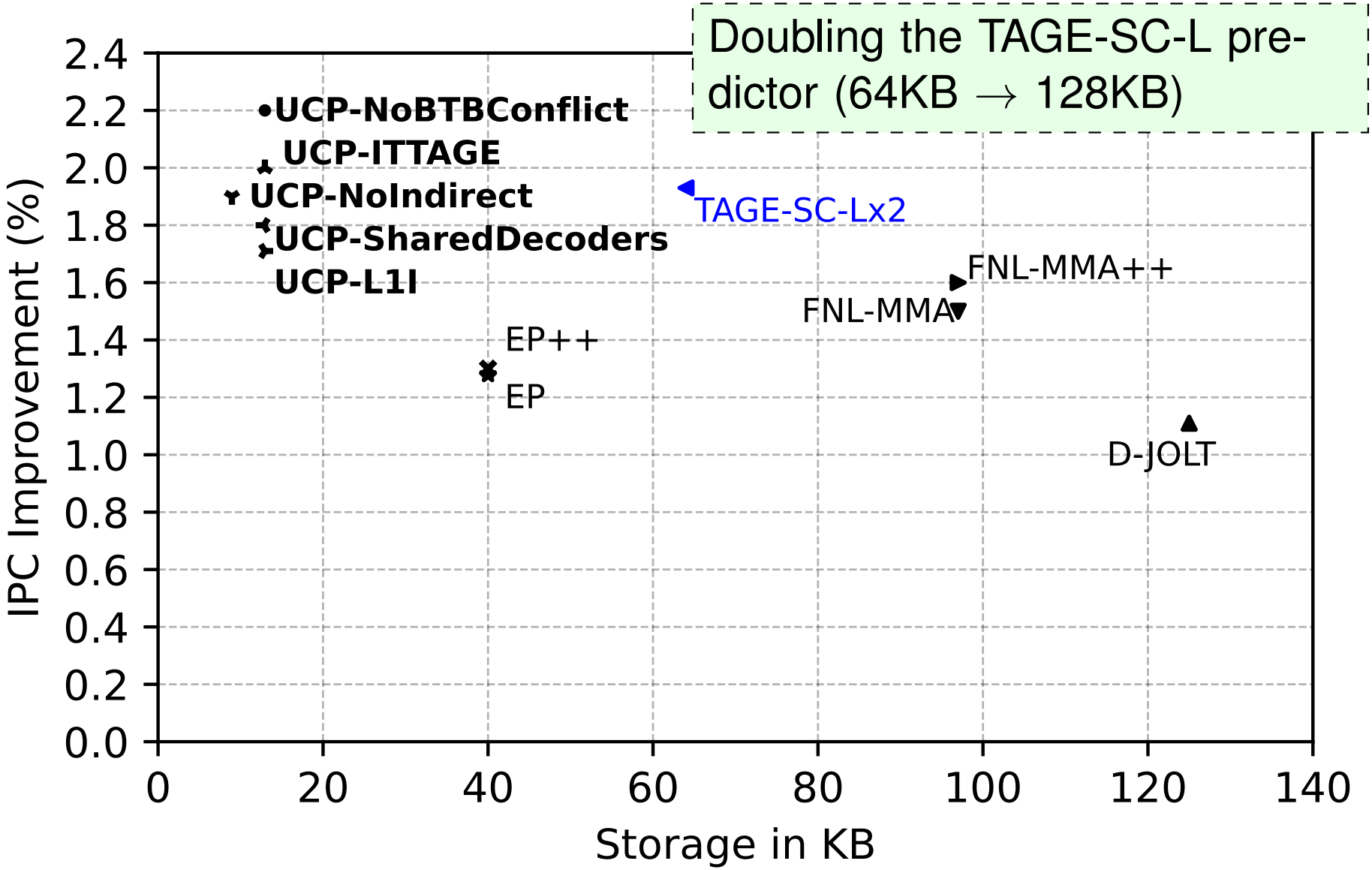

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- → UCP focus on critical instructions after a H2P branch
- → Still space for improvement in optimizing μ-op cache

ALTERNATE PATH μ-OP CACHE PREFETCHING

Sawan Singh[1] Arthur Perais[2] Alexandra Jimborean[1]
Alberto Ros[1]

singh.sawan@um.es

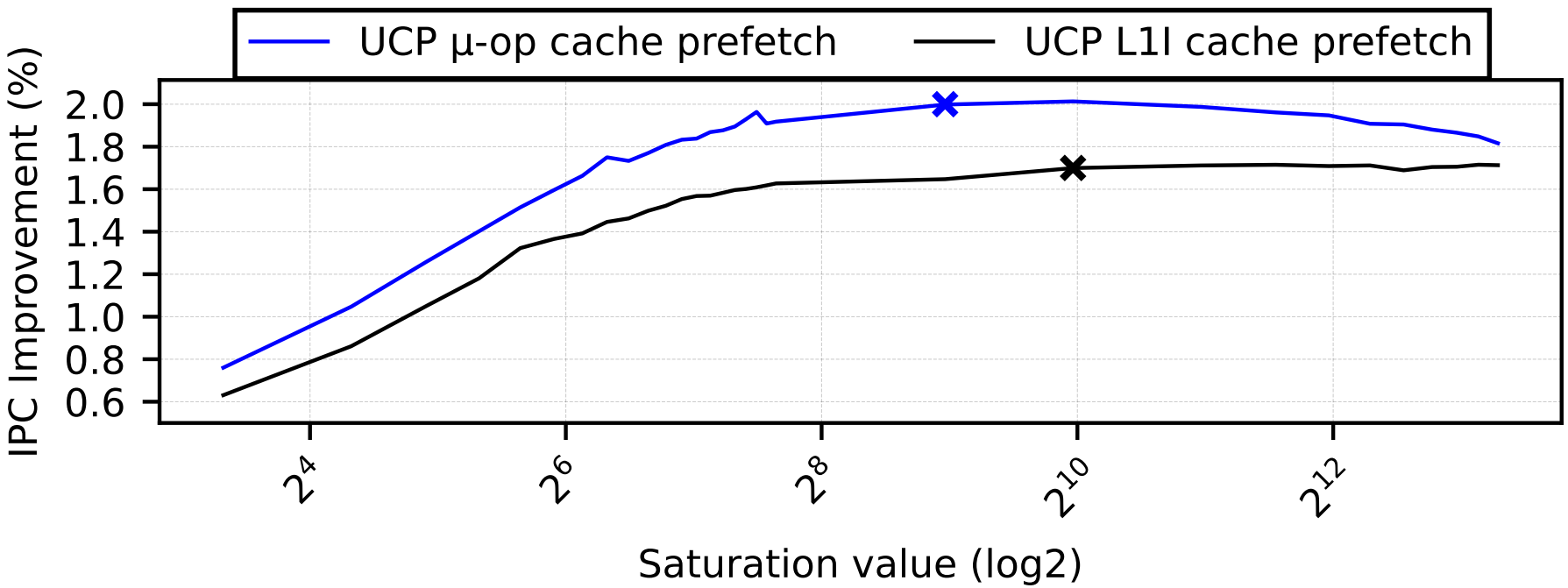
Thank you for your attention!

ECHO, ERC Consolidator Grant (No 819134)

BACKUP SLIDES[BTB BANKING]

- → UCP reuses the BTB by doubling the number of BTB banks (from 16 to 32)
- → Each cycle we determine the banks to be accessed
- → By default, demand requests are given priority to access the conflict banks
- → UCP keeps a 3-bit saturated counter which is incremented every time the alternate path is delayed
- → When the counter saturates, the alternate path is given priority for the conflict banks in that cycle
- → The counter resets next cycle

BACKUP SLIDES[SATURATION COUNTER]



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